

# MS-7680

m-ATX Ver: 10

## CPU:

INTEL - Sandy Bridge LGA 1155

## System Chipset:

INTEL - Cougar Point PCH

## OnBoard Chipset:

HD Audio Codec:RTL887

LAN:RTL 8111E 10/100/1000

SIO:FIN71889AD

Flash ROM: 64Mb SPI (PCH)

## Main Memory:

DDRIII (1066/1333MHz) \* 2 (Dual Channel)

## Expansion Slots:

PCI Express (X16) Slot \* 1

PCI Express (X1) Slot \* 3

## PWM:

Controller:VRD12 UPI6234 3+1+1+1-Phase

CPU+GPU

Controller:uP6234

CPU VTT CPU SA

Controller:uP6103

DDR PCH

## ACPI:

UPI

## Other:

SATA3.0 x2 + SATA2.0 x4 (PCH)

USB2.0 RearX6 Front x8

D-SUB \*1

DVI-D PORT\*1

HDMI \*1

TPM Header \*1

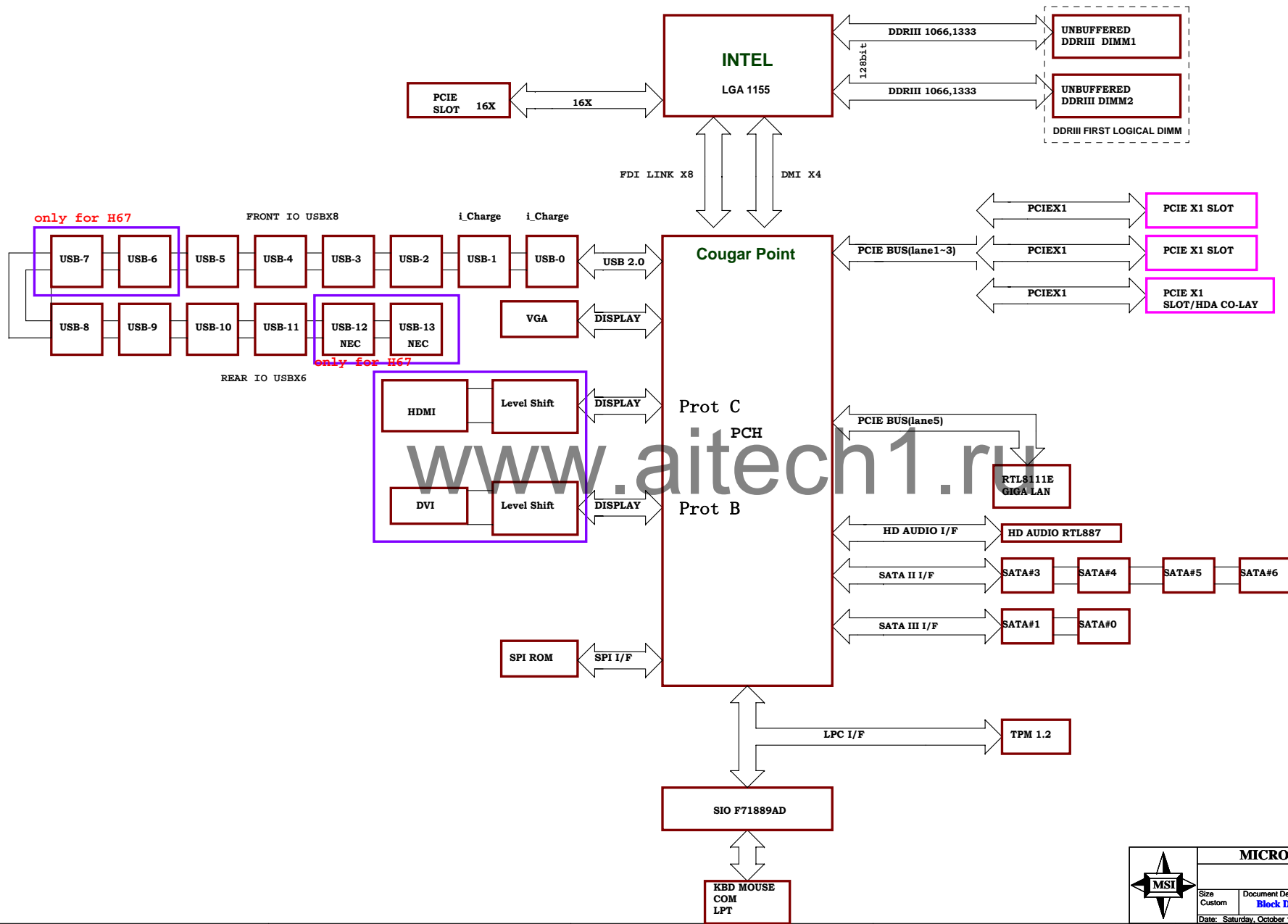
COM Header \*1

LPT Header \*1

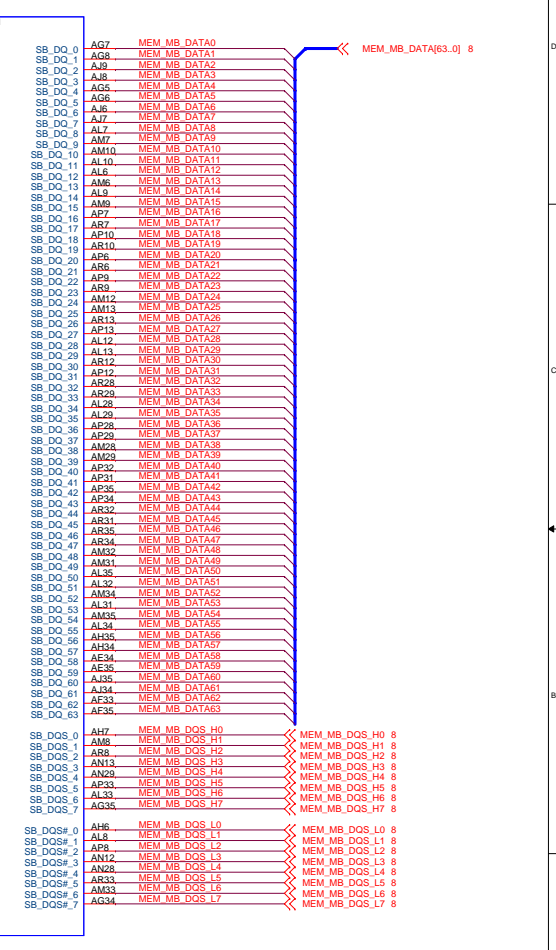
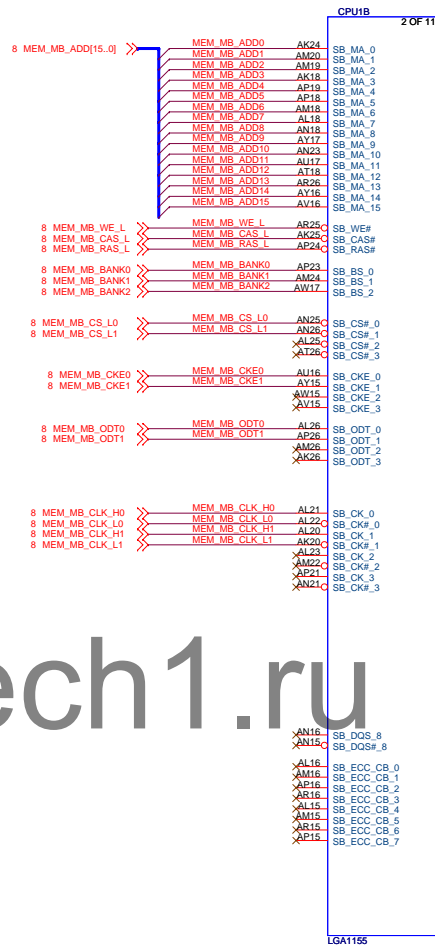
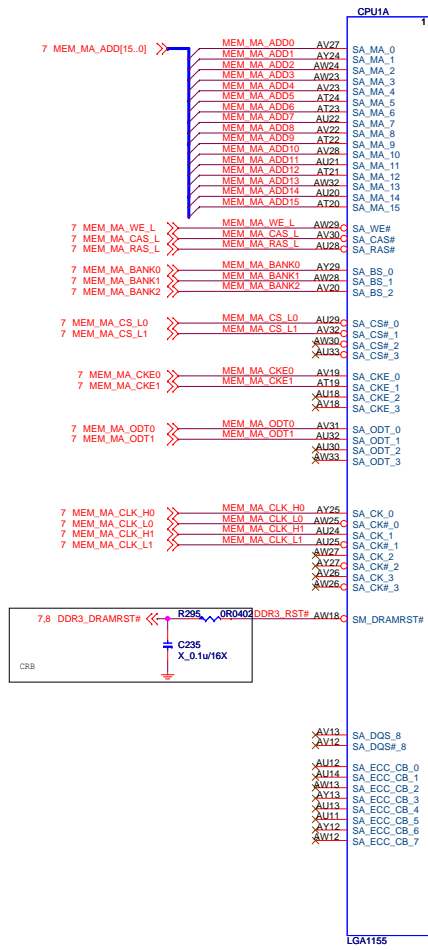
on BOARD BUZZER

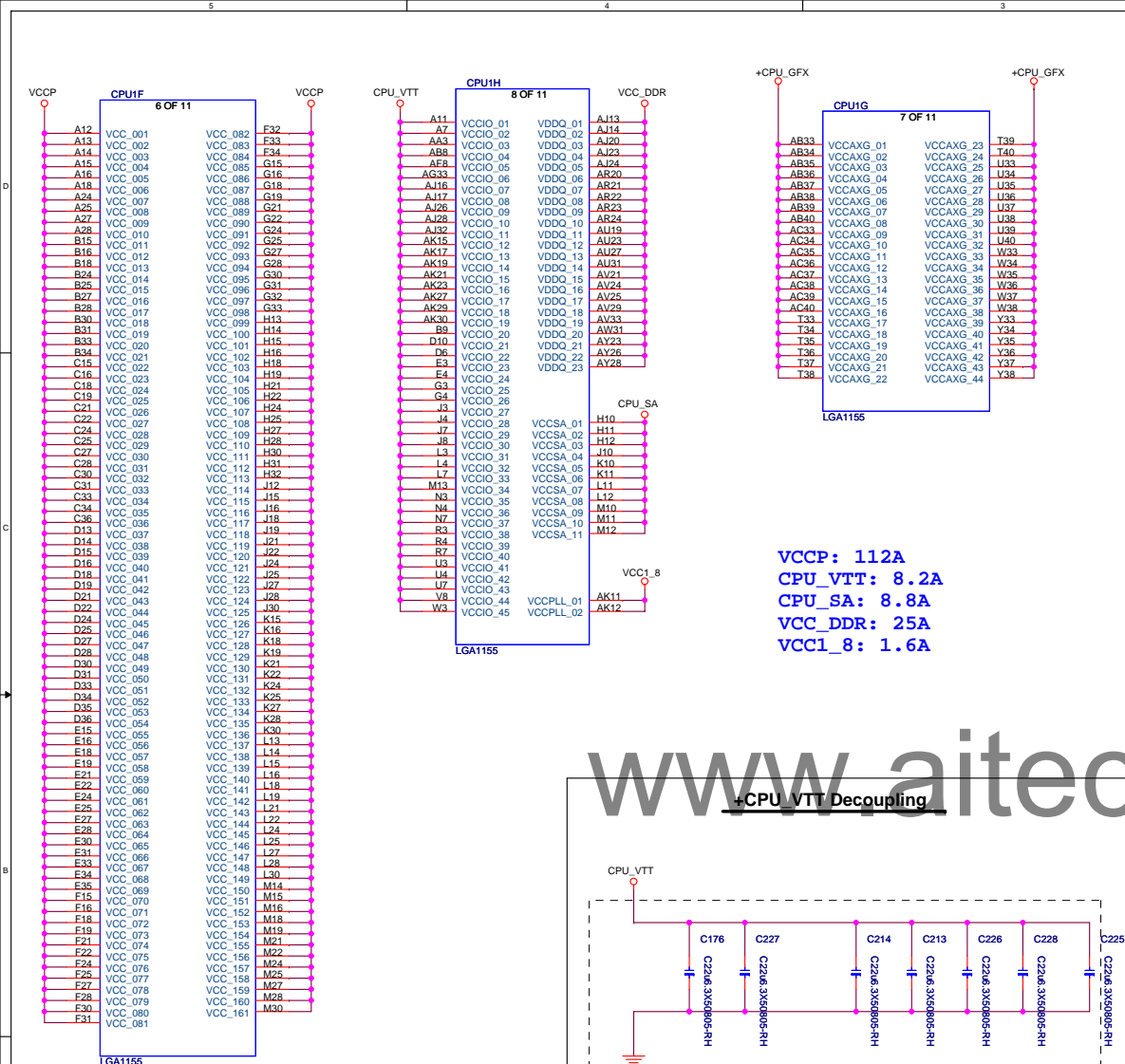
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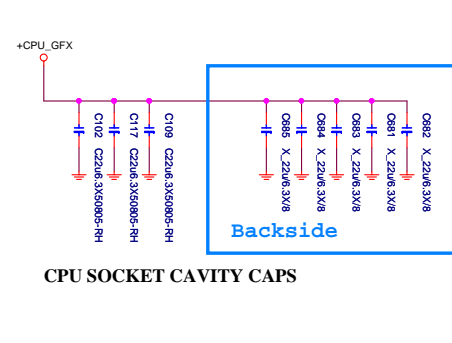




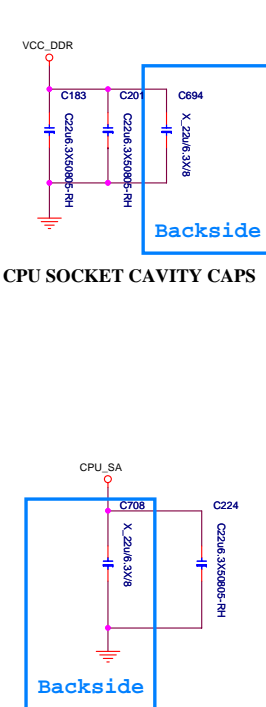




## +CPU\_GFX Decoupling

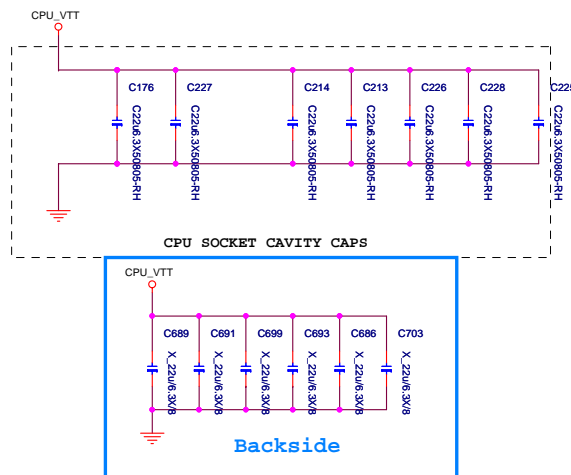


## +1.5V\_DDR3-Decoupling

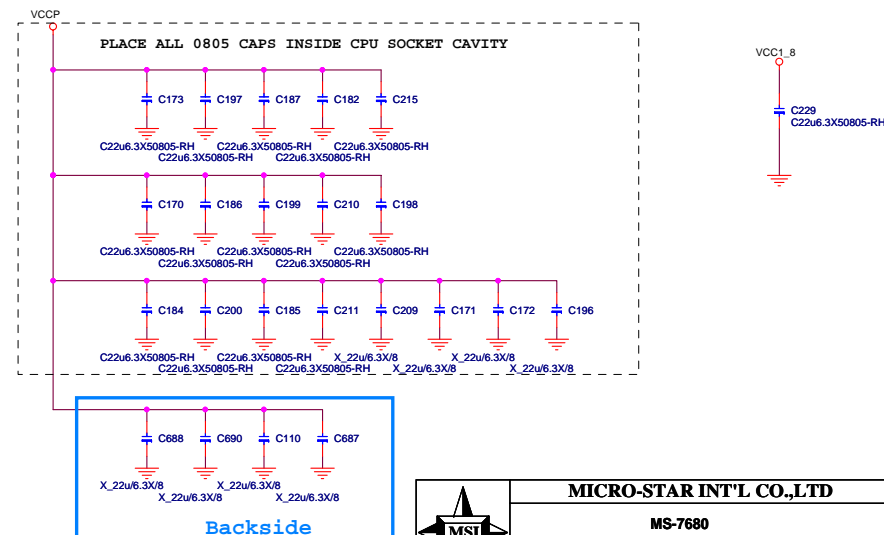


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## +CPU\_VTT Decoupling



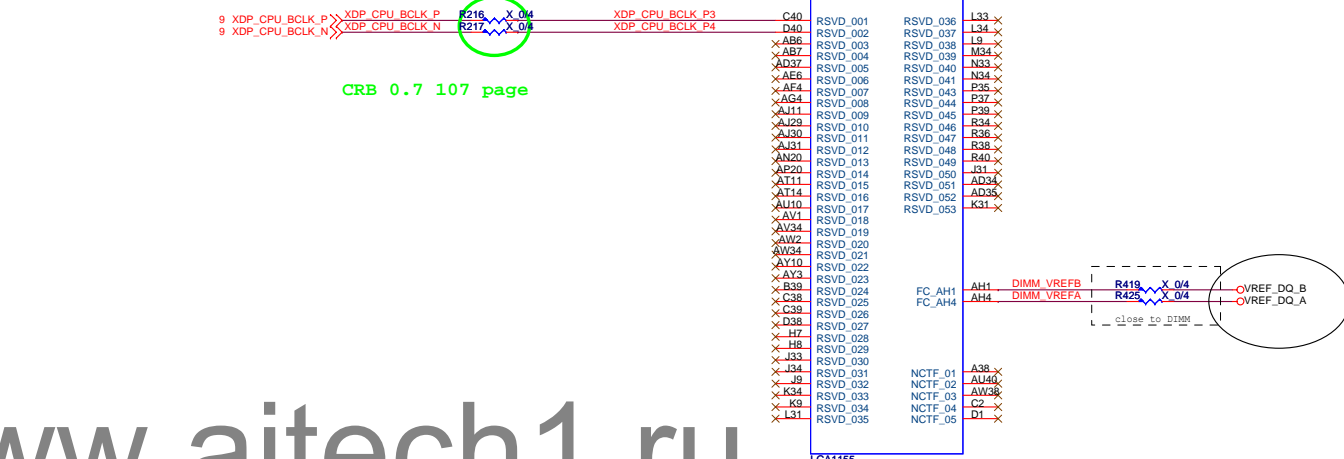
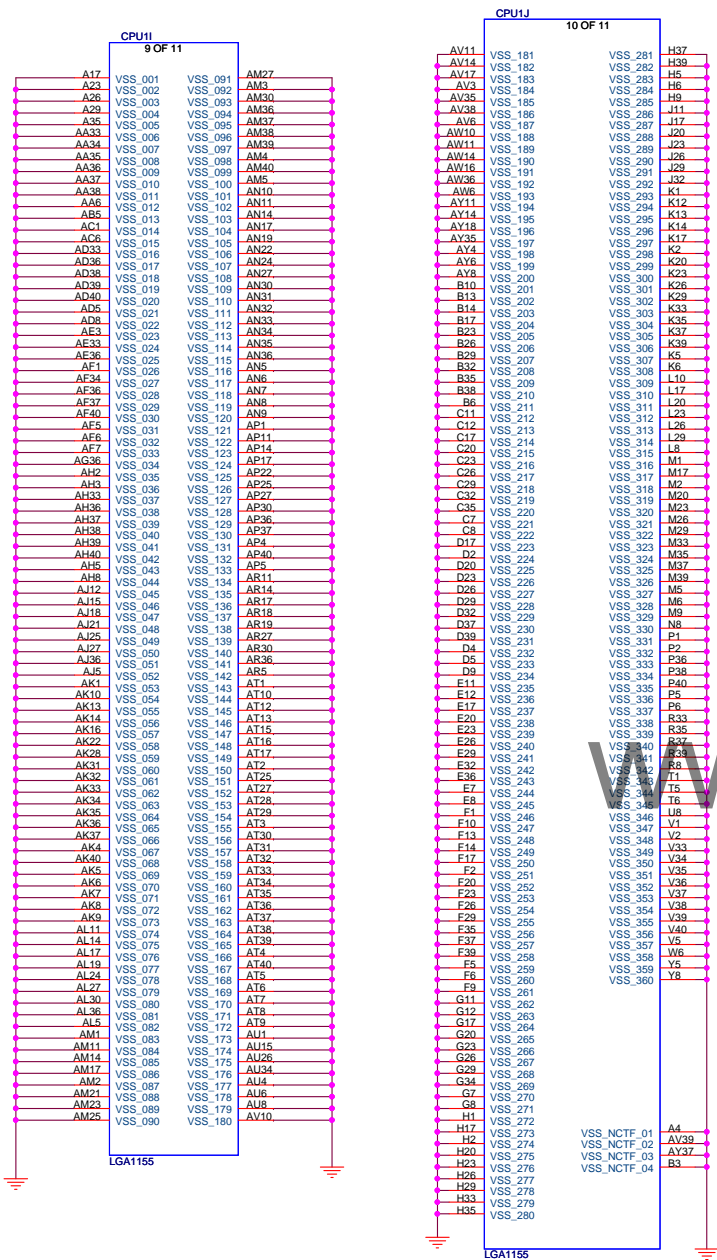
## +CPU\_VCCP-Decoupling



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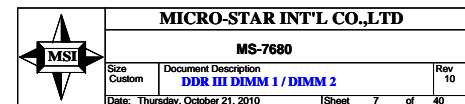
**MS-7680**

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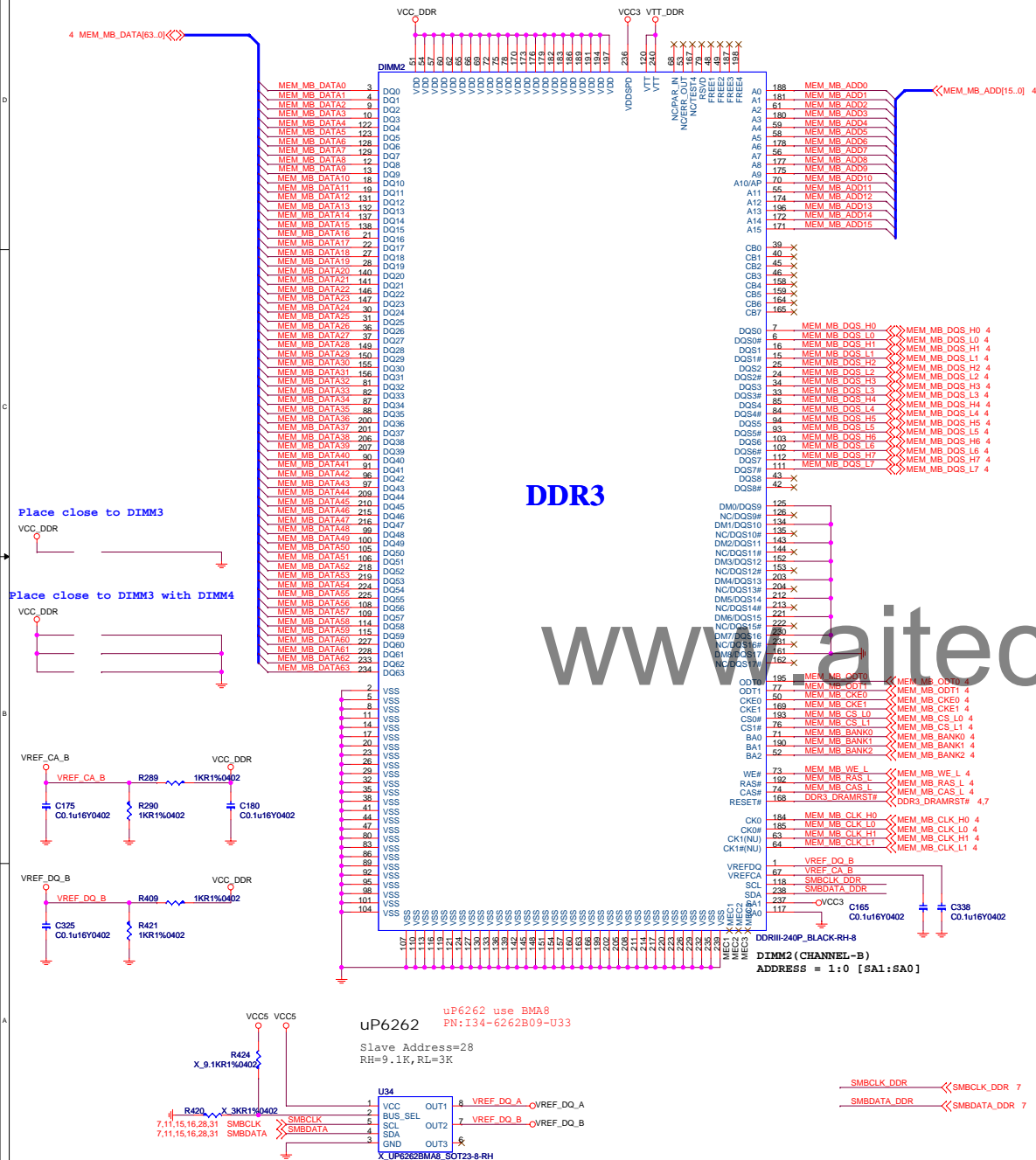
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## DDRIII DIMM\_A1



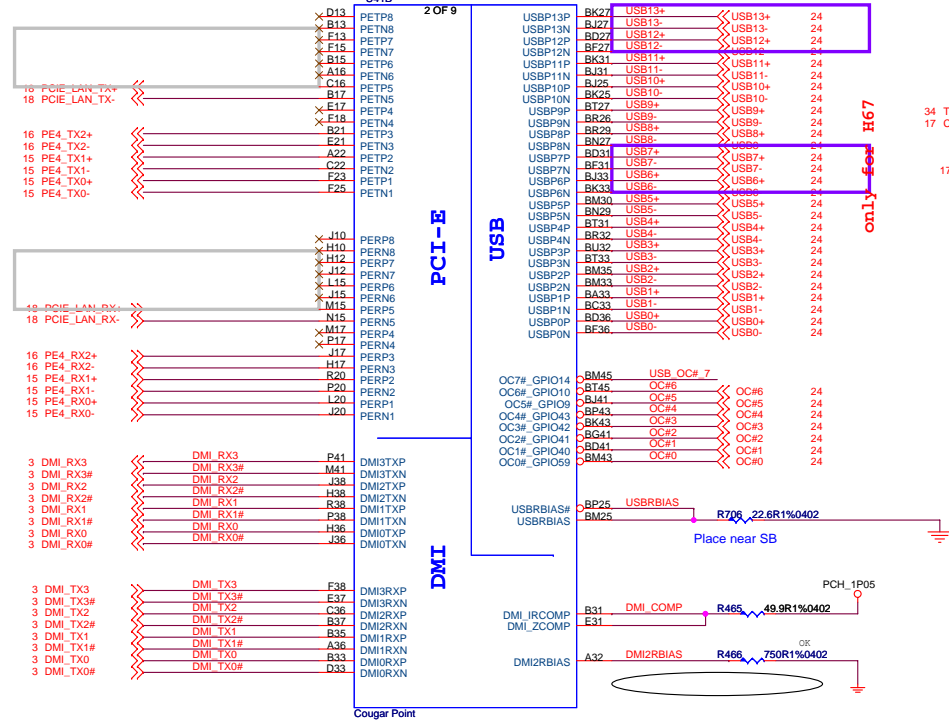


# DDR3 DIMM\_B0





H61 PCIe ports 7 and 8 are disabled



Programable output clock to 48MHZ

no clock gen pull down

Backside

0831 Lencho change to 5010



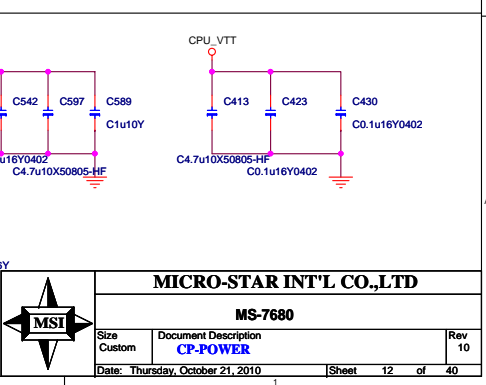
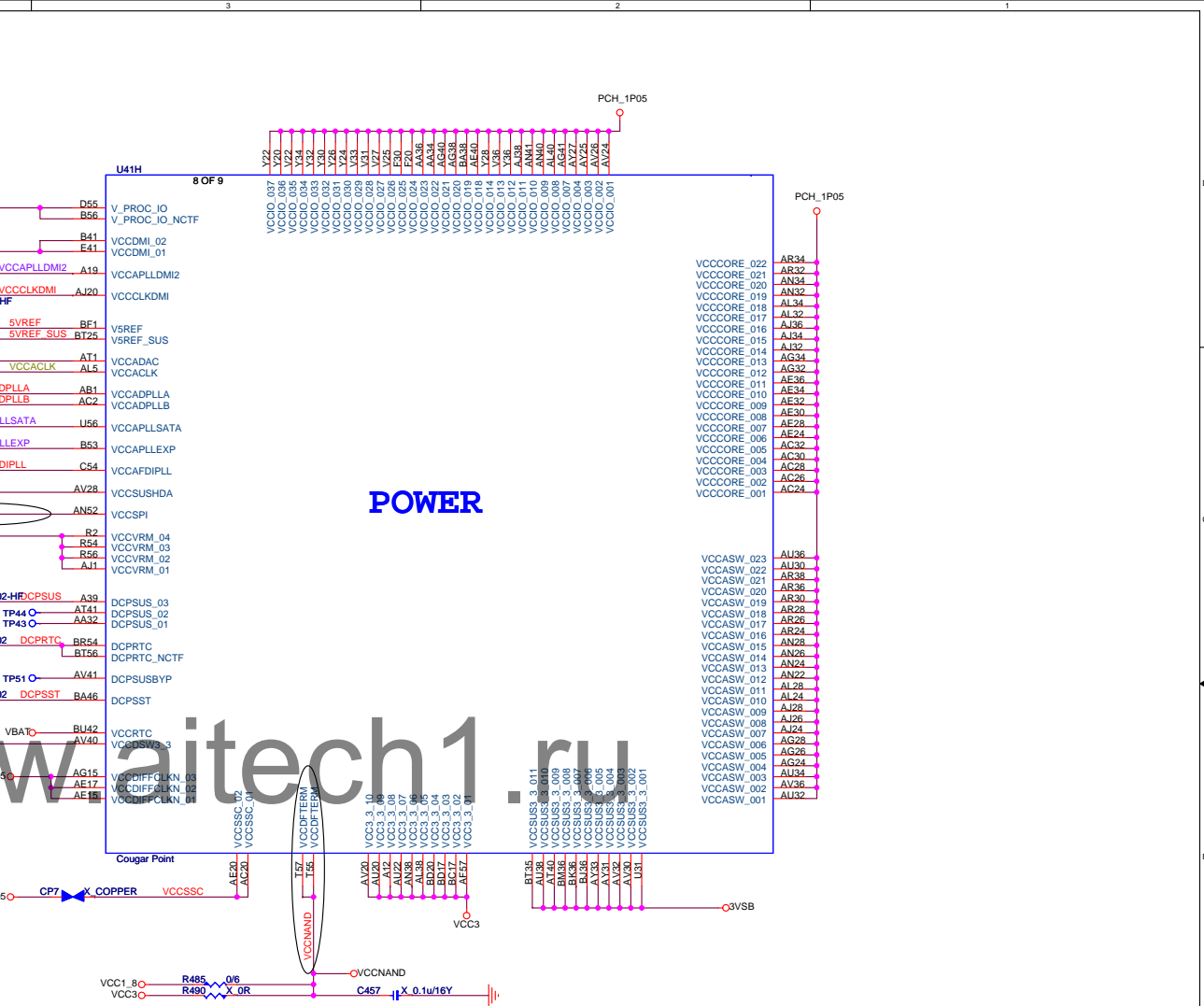
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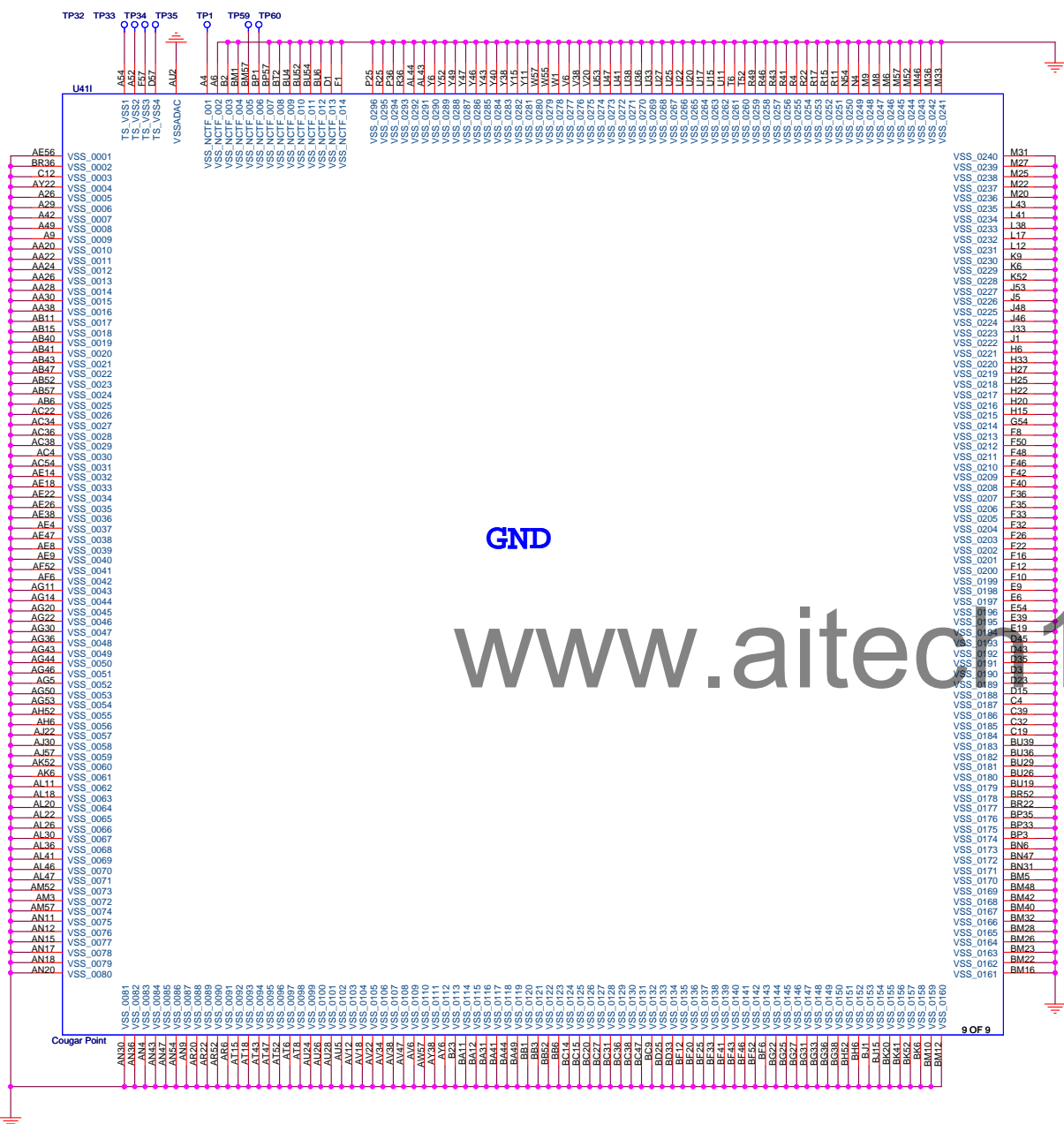
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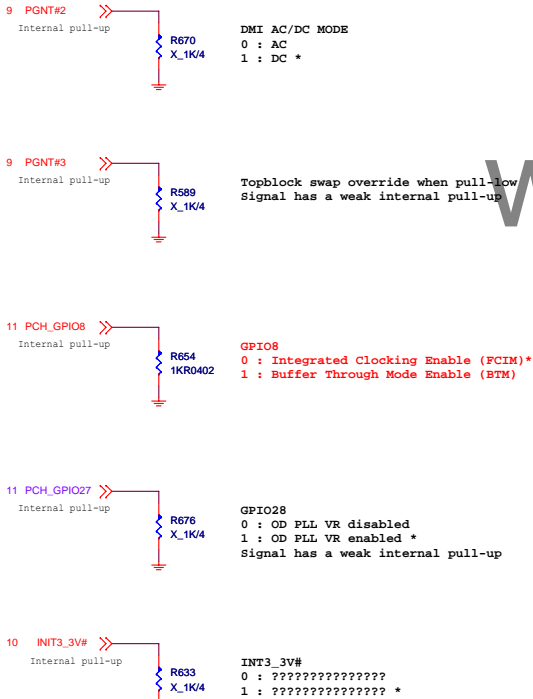
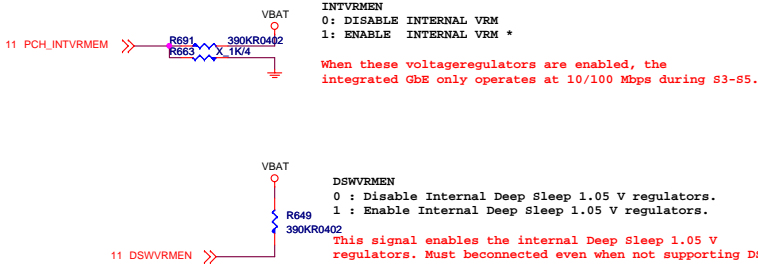
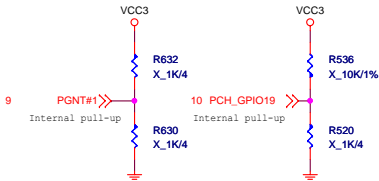




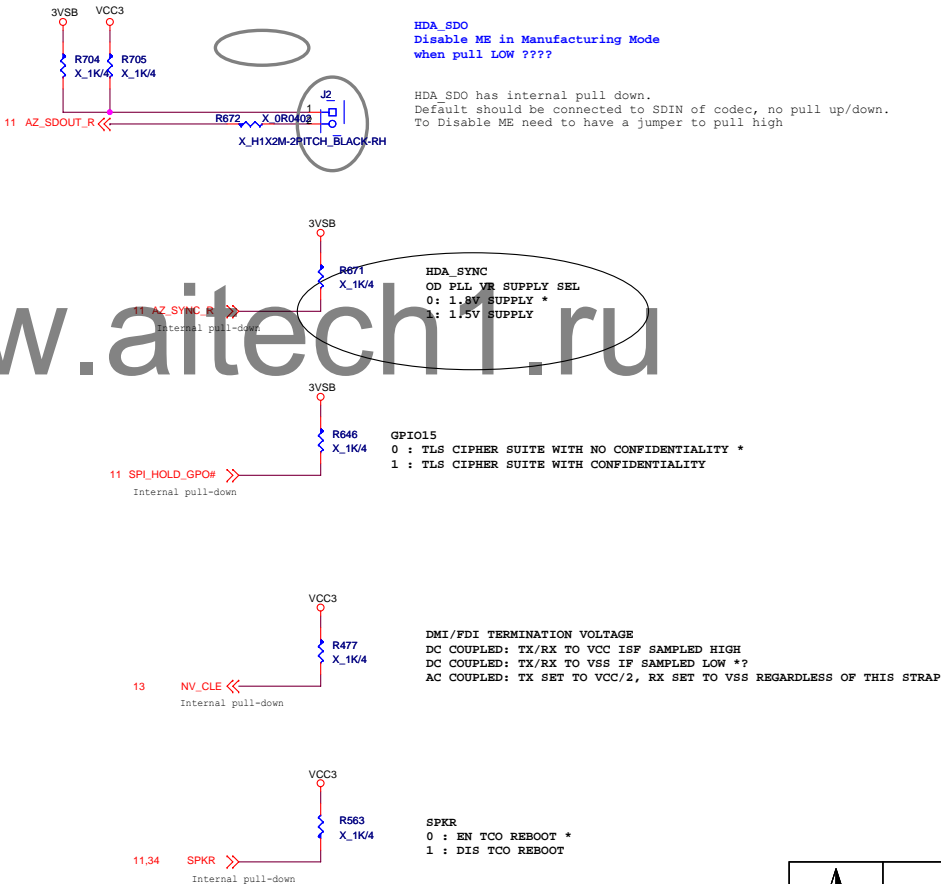


PCH Straps

BOOT DEVICE	GNT1	SATA1GP/GPIO19
LPC	0	0
PCI	1	0
SPI	1	1



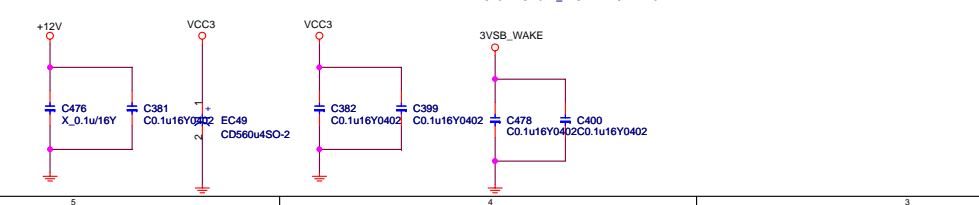
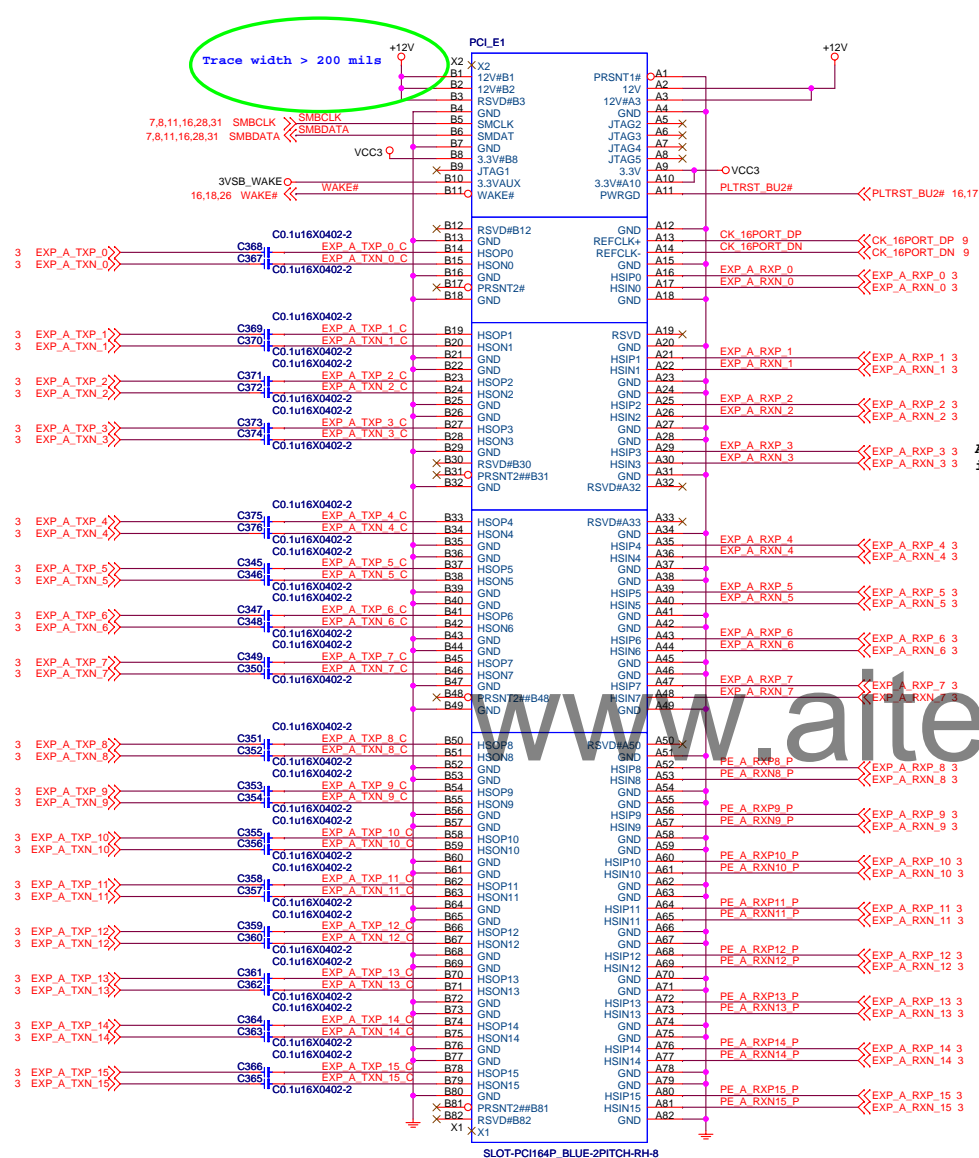
1: INIT3\_3V to asserted for 16 PCI clock to reset the processor by some evens occur.  
0: Can not to reset the processor.



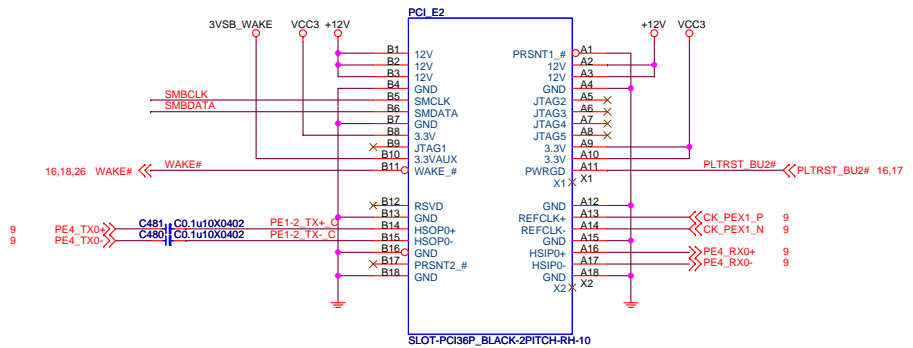
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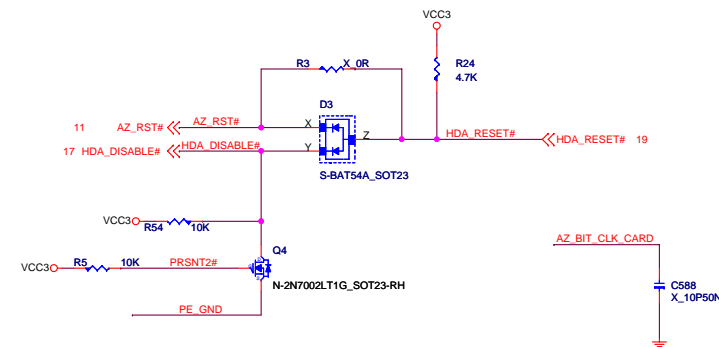
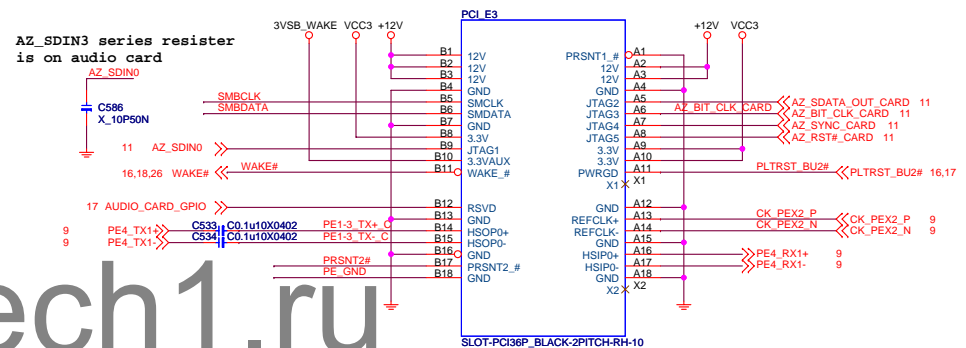
PCI\_Express X16 slot



**PCI EXPRESS x1-PORT**



**PCI EXPRESS x1-PORT**



```
HDA_DISABLE#:
to SIO GPI053 ,pin18
Hi: onboard codec Verb table
Low: PCIE Audio Verb table
```

	PE1X1_PRSENT#	PE_GND
Other board	0	0
4132 audio	1	0
N/A	1	N/C



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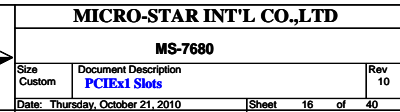
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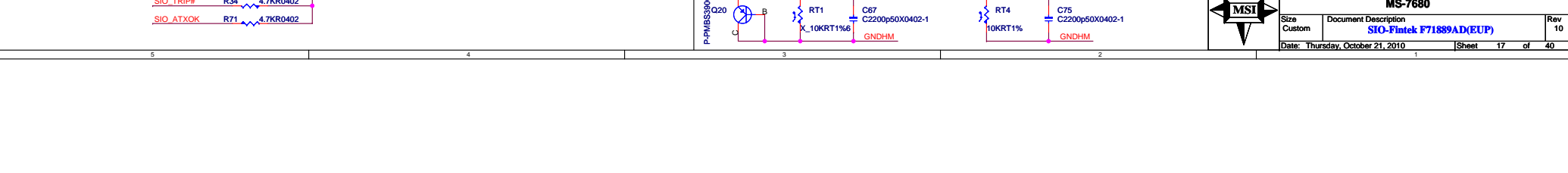
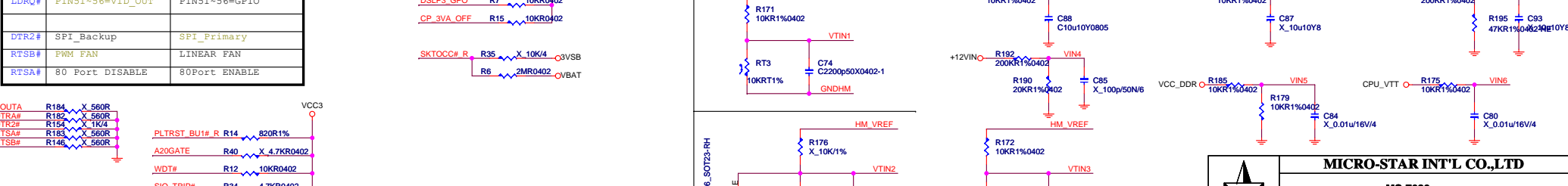
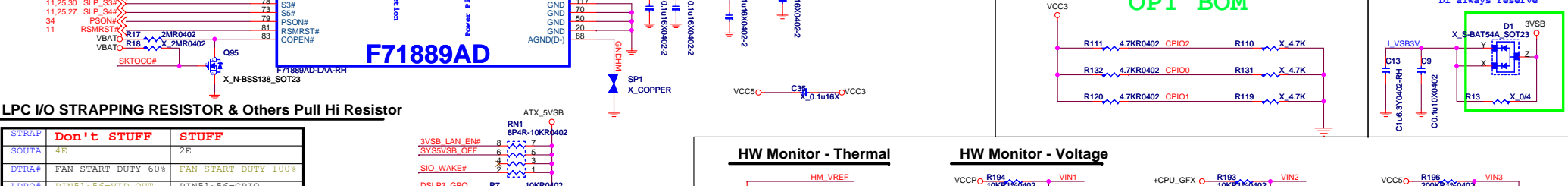
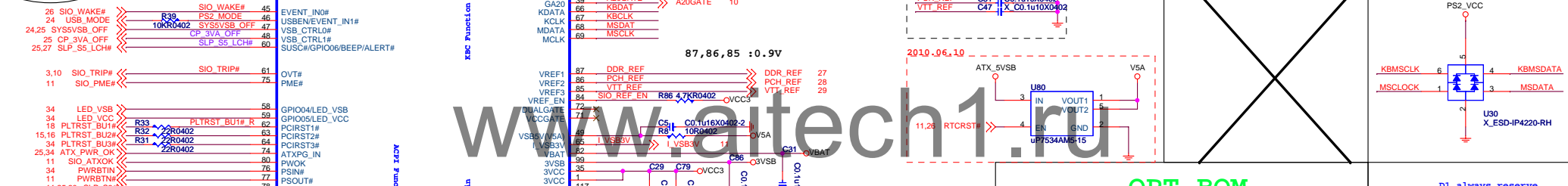
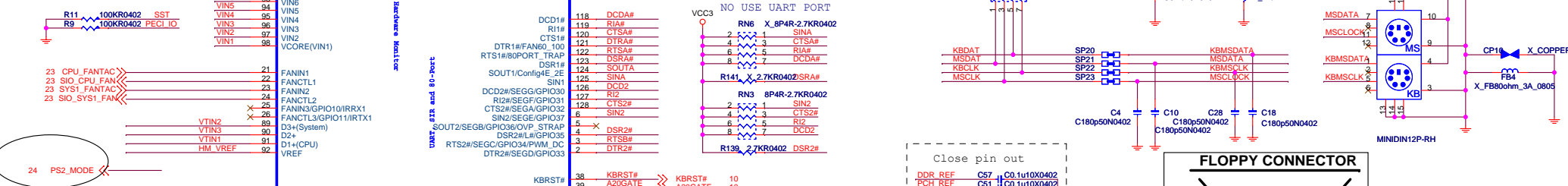
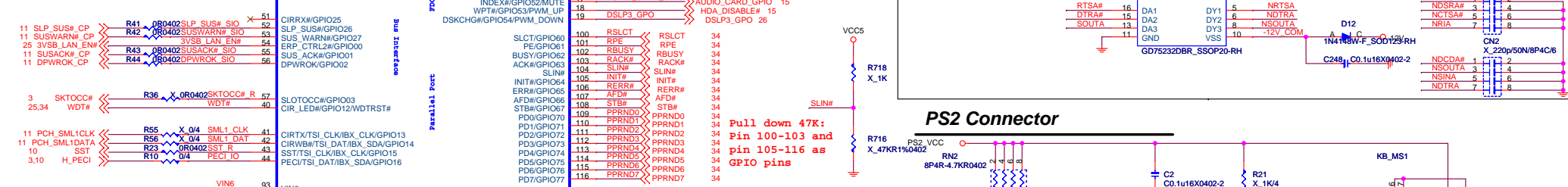
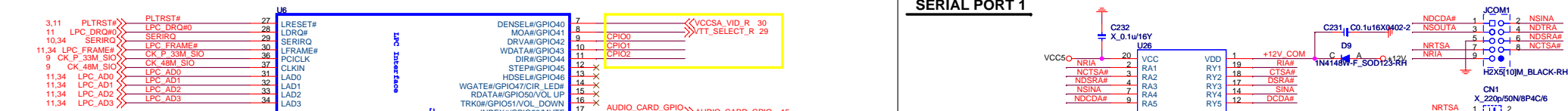


The diagram illustrates the electrical connections for the PCI-E4 connector. It shows the mapping of signals from the system components to the specific pins of the connector. Key connections include:

- Power and Ground:**
  - 3VSB\_WAKE** and **VCC3 +12V** are connected to pins **B1**, **B2**, **B3**, **B4**, **B5**, **B6**, **B7**, **B8**, **B9**, **B10**, and **B11**.
  - 12V** is connected to pins **B1**, **B2**, **B3**, **B4**, **B5**, **B6**, **B7**, **B8**, **B9**, **B10**, and **B11**.
  - GND** is connected to pins **B1**, **B2**, **B3**, **B4**, **B5**, **B6**, **B7**, **B8**, **B9**, **B10**, and **B11**.
  - 3.3V** is connected to pins **B10** and **B11**.
  - 3.3V\_AUX** is connected to pin **B10**.
  - WAKE\_#** is connected to pin **B11**.
- Data and Control:**
  - SMBCLK** and **SMBDATA** are connected to pins **B1**, **B2**, **B3**, **B4**, **B5**, **B6**, **B7**, **B8**, **B9**, **B10**, and **B11**.
  - RSVD** is connected to pins **B12**, **B13**, **B14**, **B15**, **B16**, **B17**, and **B18**.
  - GND** is connected to pins **B12**, **B13**, **B14**, **B15**, **B16**, **B17**, and **B18**.
  - HSOP0+** and **HSOP0-** are connected to pins **B12**, **B13**, **B14**, **B15**, **B16**, **B17**, and **B18**.
  - PRSTNT2\_#** is connected to pin **B18**.
- Other Signals:**
  - PRSTNT1\_#** is connected to pin **A1**.
  - A2**, **A3**, **A4**, **A5**, **A6**, **A7**, **A8**, **A9**, **A10**, **A11**, **A12**, **A13**, **A14**, **A15**, **A16**, **A17**, and **A18** are connected to pins **A1**, **A2**, **A3**, **A4**, **A5**, **A6**, **A7**, **A8**, **A9**, **A10**, **A11**, **A12**, **A13**, **A14**, **A15**, **A16**, **A17**, and **A18**.
  - PLTRST\_BU2#** is connected to pin **A11**.
  - CK\_PEX\_4X\_P** and **CK\_PEX\_4X\_N** are connected to pins **A12**, **A13**, **A14**, **A15**, **A16**, **A17**, and **A18**.
  - PE4\_RX2+** and **PE4\_RX2-** are connected to pins **A12**, **A13**, **A14**, **A15**, **A16**, **A17**, and **A18**.

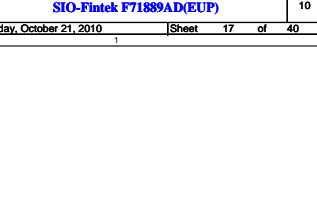
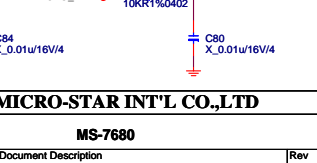
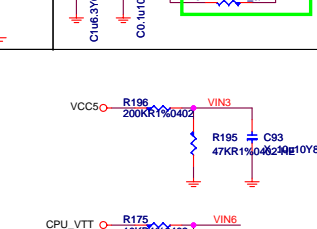
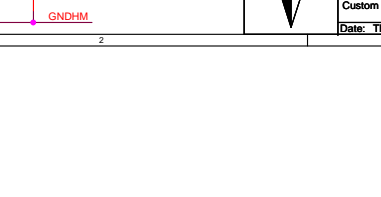
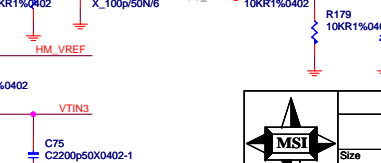
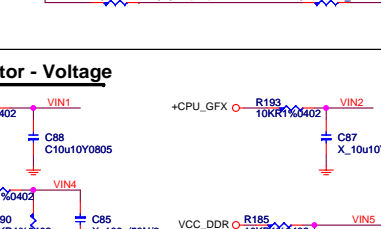
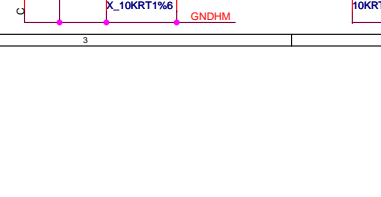
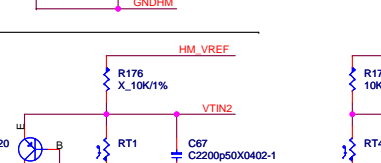
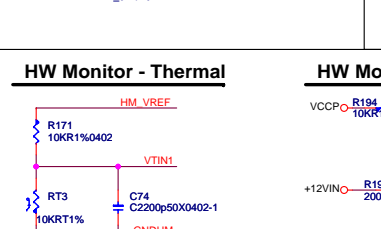
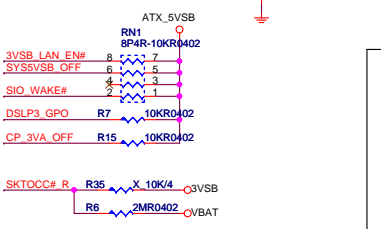
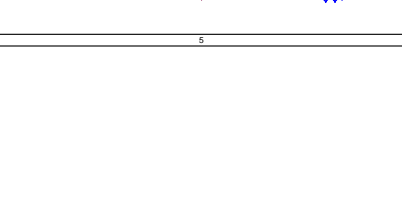
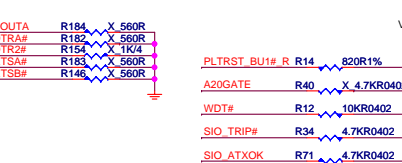
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[illegible]



LPC I/O STRAPPING RESISTOR & Others Pull Hi Resistor

STRAP	Don't STUFF	STUFF
SOUTA	4E	2E
DTRA#	FAN START DUTY 60%	FAN START DUTY 100%
LDRQ#	PIN51-56=VID_OUT	PIN51-56=GPIO
DTR2#	SPI_Backup	SPI_Primary
RTSA#	PWM FAN	LINEAR FAN
RTSA#	80 Port DISABLE	80Port ENABLE

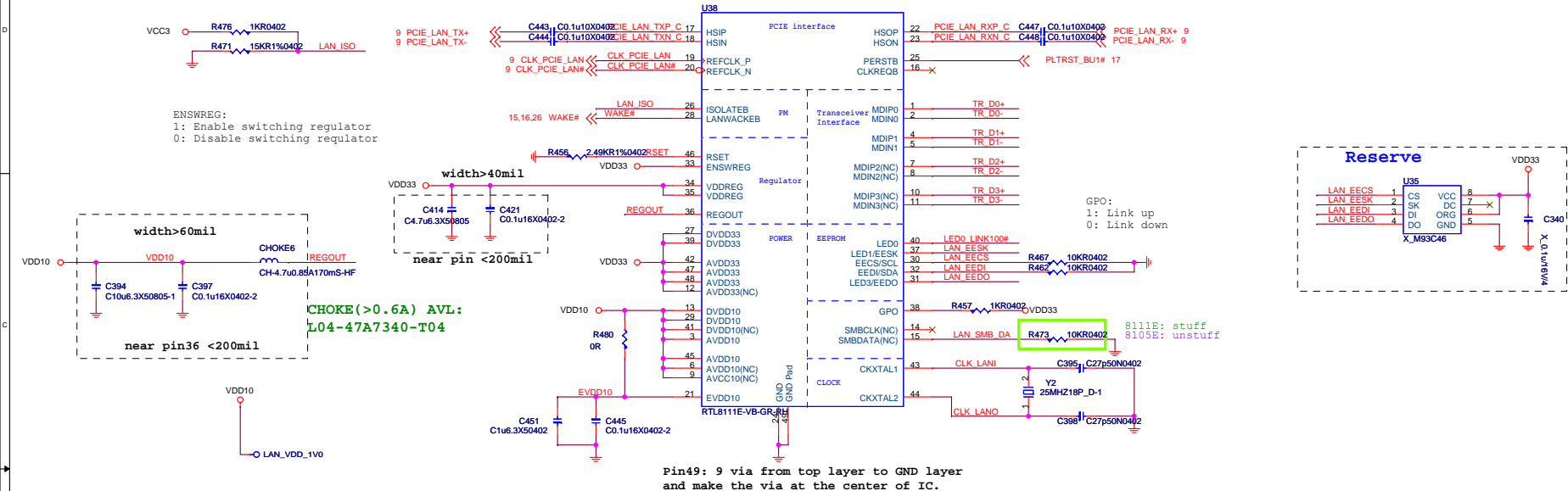




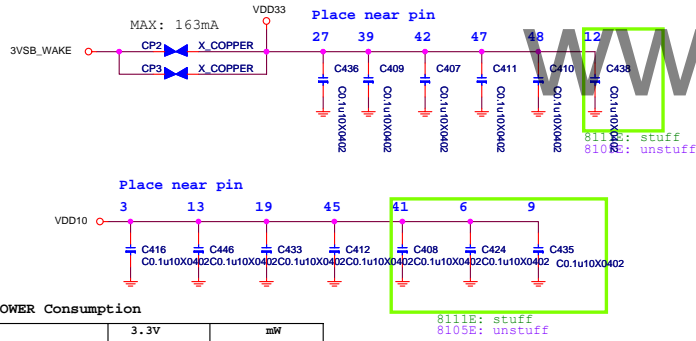
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**MS-7680**  
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**SIO-Fintek F71889AD(EUP)**  
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# RTL8111E Giga LAN

## RTL8105E 10/100M LAN



3.3v Power on rise time : 1-100ms.



8105E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	14/75	46/248
100 M Idle/TxRx	43/66	142/218
80 ALDPS	3.2	11

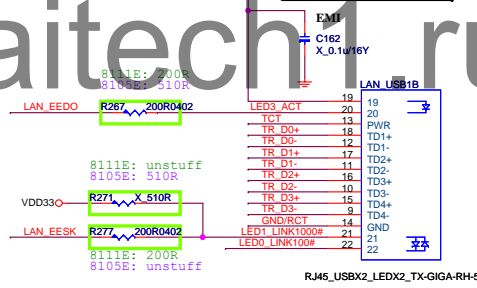
8111E POWER Consumption

	3.3V	mW
10 M Idle/TxRx	12/66	40/218
100 M Idle/TxRx	31/44	102/145
Giga Idle/TxRx	135/163	452/538
ALDPS	4	13

close to Connector

close to Connector

LAN Connector



Giga-Lan	10/100-Lan
N58-22F0731	N58-22F0771
Link Yellow	Link Yellow
Active Blinking	Active Blinking
1000 Orange	1000 Orange
100 Green	100 Green
10 None	10 None
19	19
20	20
21	21
22	22



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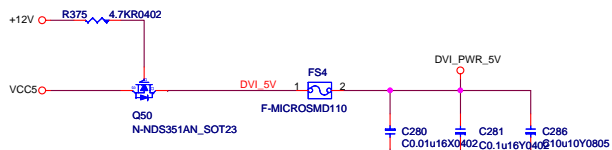
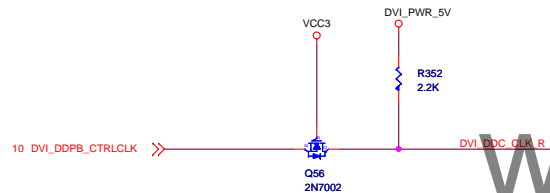
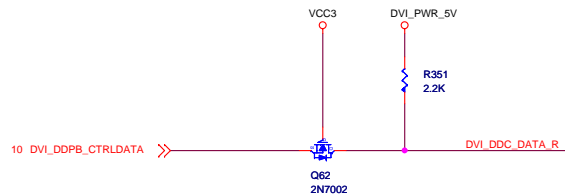
MS-7680

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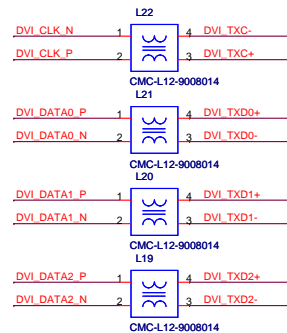
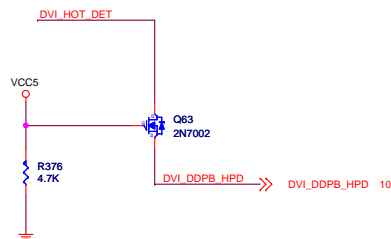
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## ALC892

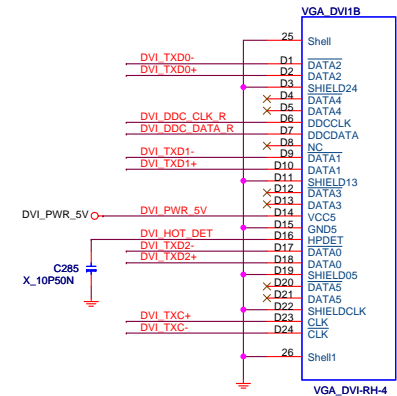
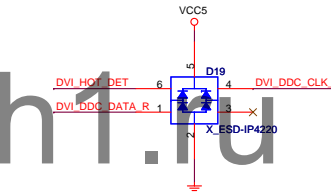
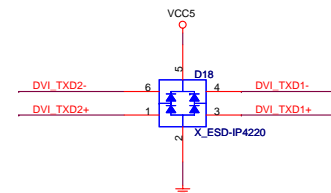
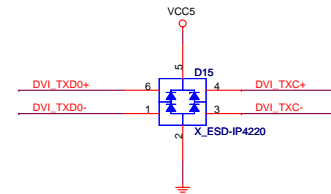
# DVI level shifter



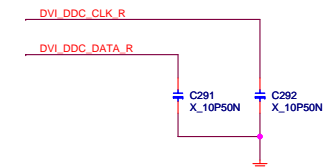
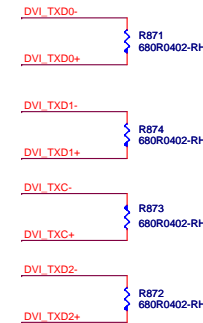
High/Low Detect



reserve



For EMI



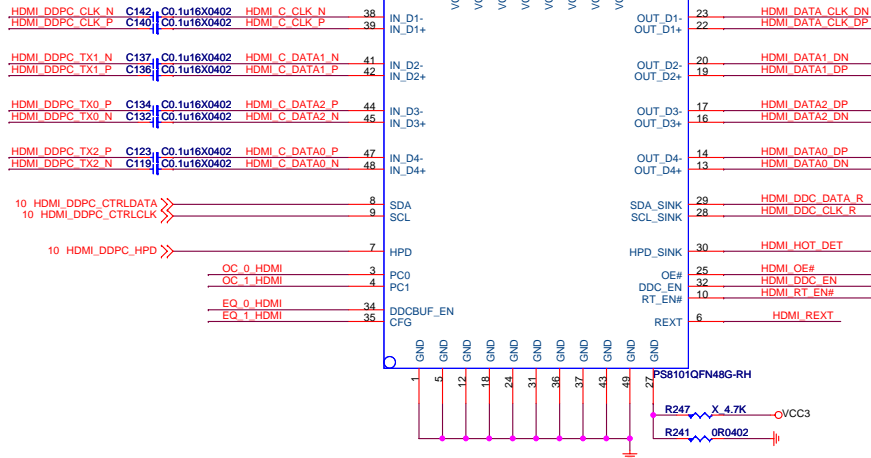
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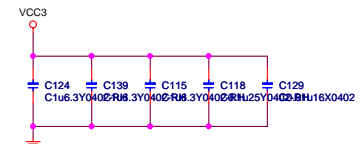
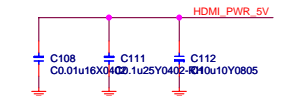
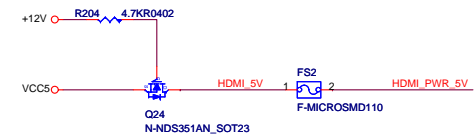
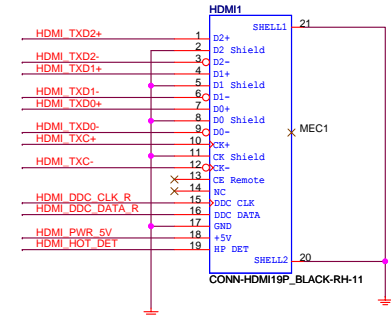
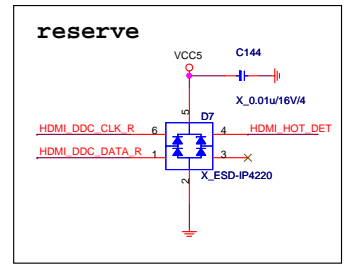
Size	Document Description	Rev
Custom	DVI transfer	10
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# HDMI level shifter

10 HDMI\_DDPCK\_CLK\_P << HDMI\_DDPCK\_CLK\_P  
10 HDMI\_DDPCK\_CLK\_N << HDMI\_DDPCK\_CLK\_N  
10 HDMI\_DDPCK\_TX2\_P << HDMI\_DDPCK\_TX2\_P  
10 HDMI\_DDPCK\_TX2\_N << HDMI\_DDPCK\_TX2\_N  
10 HDMI\_DDPCK\_TX1\_P << HDMI\_DDPCK\_TX1\_P  
10 HDMI\_DDPCK\_TX1\_N << HDMI\_DDPCK\_TX1\_N  
10 HDMI\_DDPCK\_TX0\_P << HDMI\_DDPCK\_TX0\_P  
10 HDMI\_DDPCK\_TX0\_N << HDMI\_DDPCK\_TX0\_N

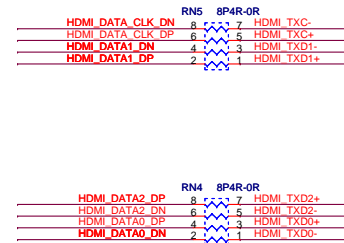
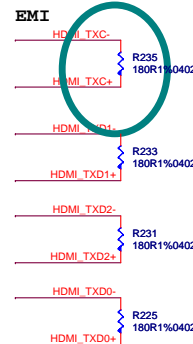


PERICOM 腹:B0B-411LS2C-P22.  
PARADE 腹:B0B-081010C-P97.



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High/Low Detect



	"0"	"1"	note
DDC_EN	DDC level shifter disable	DDC level shifter enable	internal pull-up at ~500K ohm.
RT_EN#	Input 50 ohm termination resistor enable	the input termination ; resistors are set to high impedances	internal pull-down at ~500K ohm.
OE#	enable	the chip is power down and input termination resistors will be at high impedance.	internal pull-down at ~500K ohm.
HPD_SINK	disable	enable	internal pull-down at ~200K ohm; 5V tolerant.
DDCBUF_EN	For DDC level shifting configuration, please refer to Table.		internal pull-down at ~500K ohm.
REXT			analog current generation.

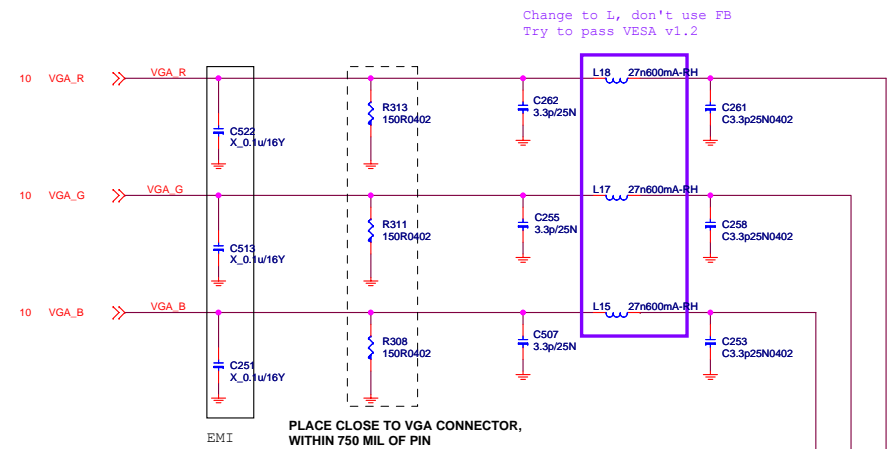
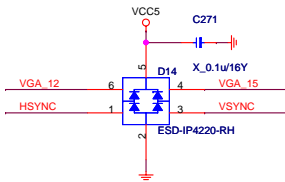
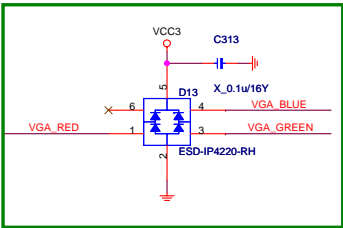
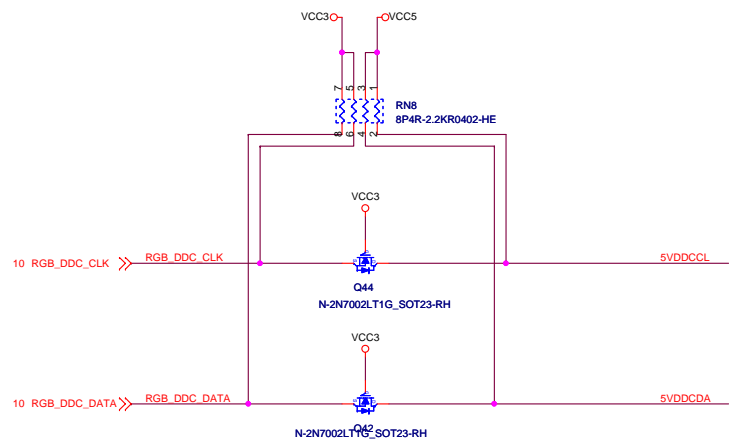
[DDC_EN, DDCBUF_EN, OE#]	DDC Passive Switch	DDC Active Buffer
1, 0, X	On	Off
1, 1, 0	Off	On
1, 1, 1	Off	Off
0, X, X	Off	Off

PC1, PC0		note
00	8 dB	internal pull-down at ~500K ohm.
01	4 dB	
10	12 dB	
11	0 dB	

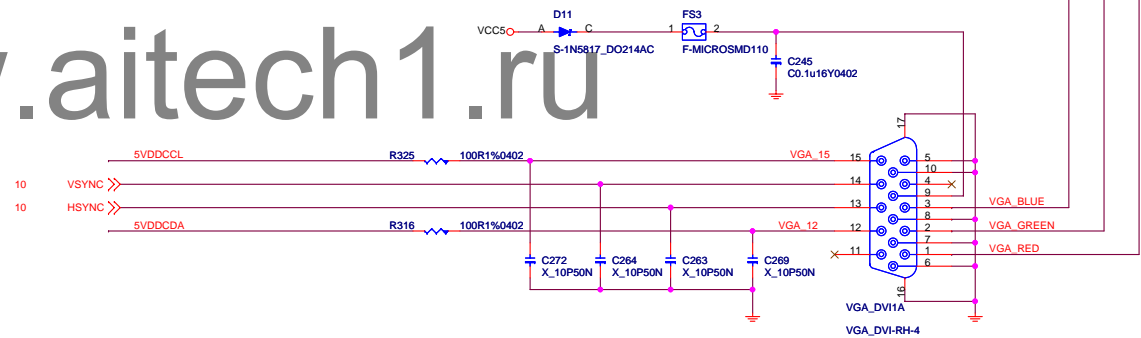
MICRO-STAR INT'L CO.,LTD		
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Size Custom	Document Description HDMI	Rev 10
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D-Sub

Level shift



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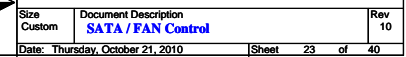
MICRO-STAR INT'L CO.,LTD		
MS-7680		
Size	Document Description	Rev
Custom	VGA	10
Date:	Thursday, October 21, 2010	Sheet 22 of 40



SATA1

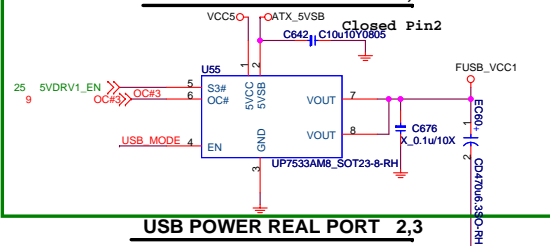


## SATA5\_6

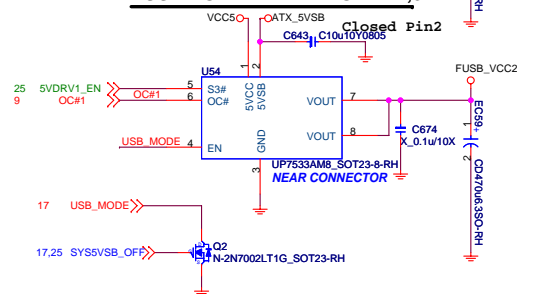


## Front USB Connector

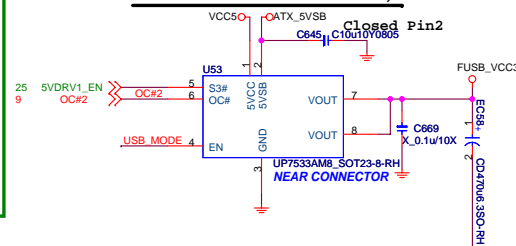
### USB POWER FOR PORT 0,1



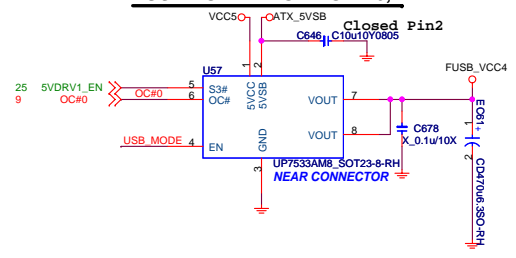
### USB POWER REAL PORT 2,3



### USB POWER FOR PORT 4,5

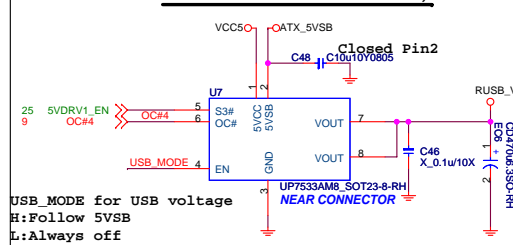


### USB POWER FOR PORT 6,7

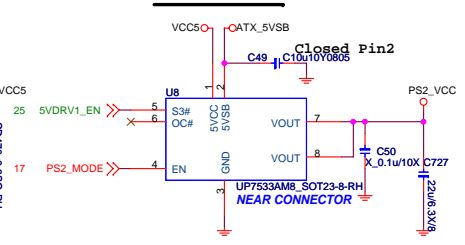


## Rear USB Connector

### USB POWER FOR PORT 6,7



### PS2 POWER

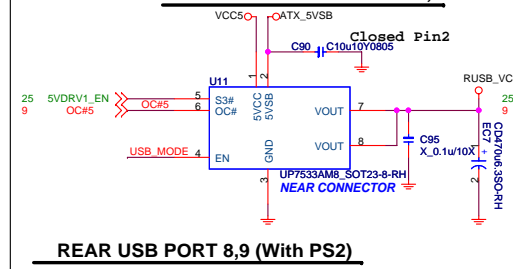


USB\_MODE for USB voltage

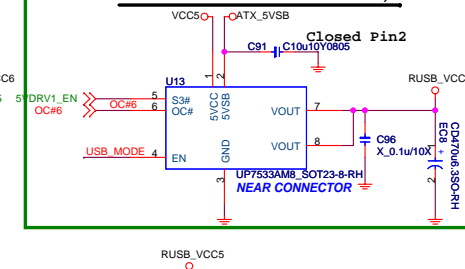
H: Follow 5VSB

L: Always off

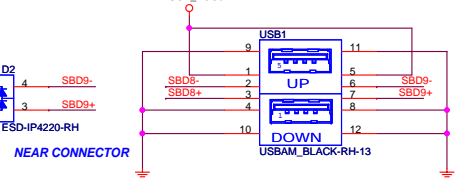
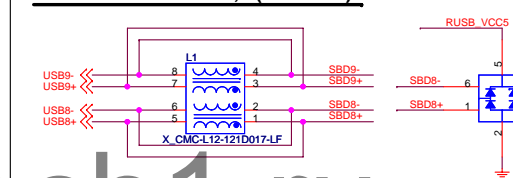
### USB POWER FOR PORT 8,9



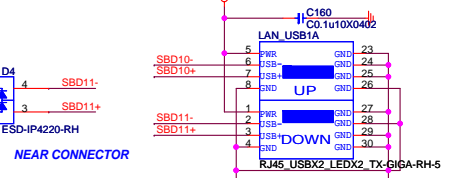
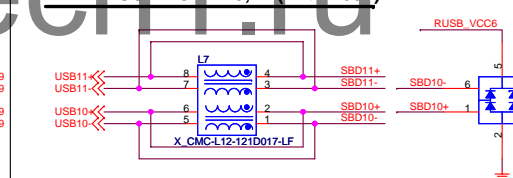
### USB POWER FOR PORT 8,9



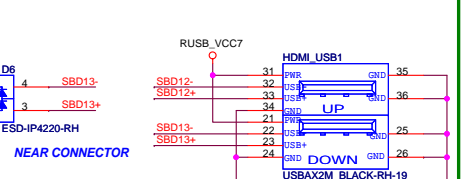
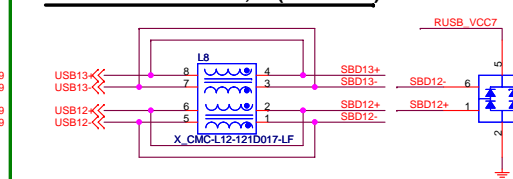
### REAR USB PORT 8,9 (With PS2)



### REAR USB PORT 10,11 (With 1394)

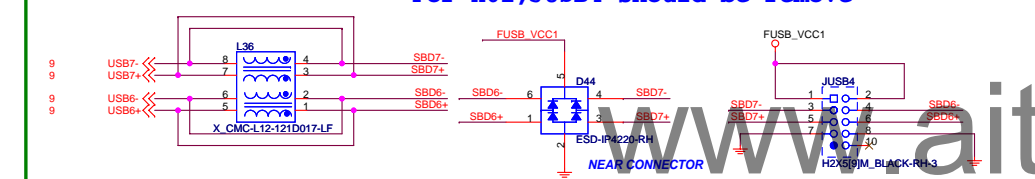


### REAR USB PORT 10,11 (With 1394)

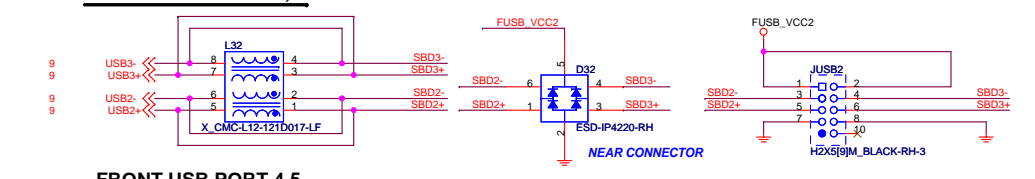


### FRONT USB PORT 0,1

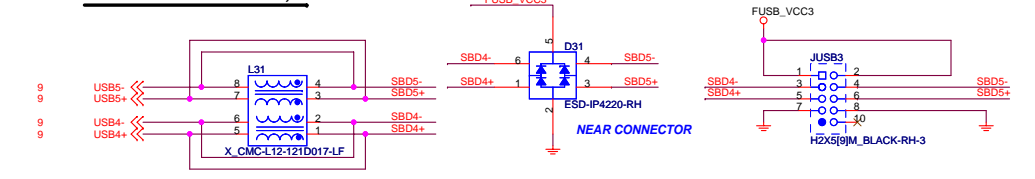
For H61, JUSB4 should be remove



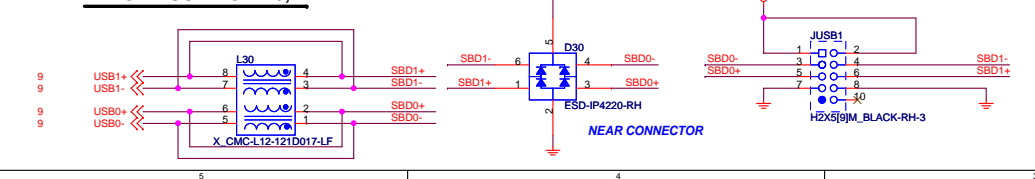
### FRONT USB PORT 2,3



### FRONT USB PORT 4,5



### FRONT USB PORT 6,7



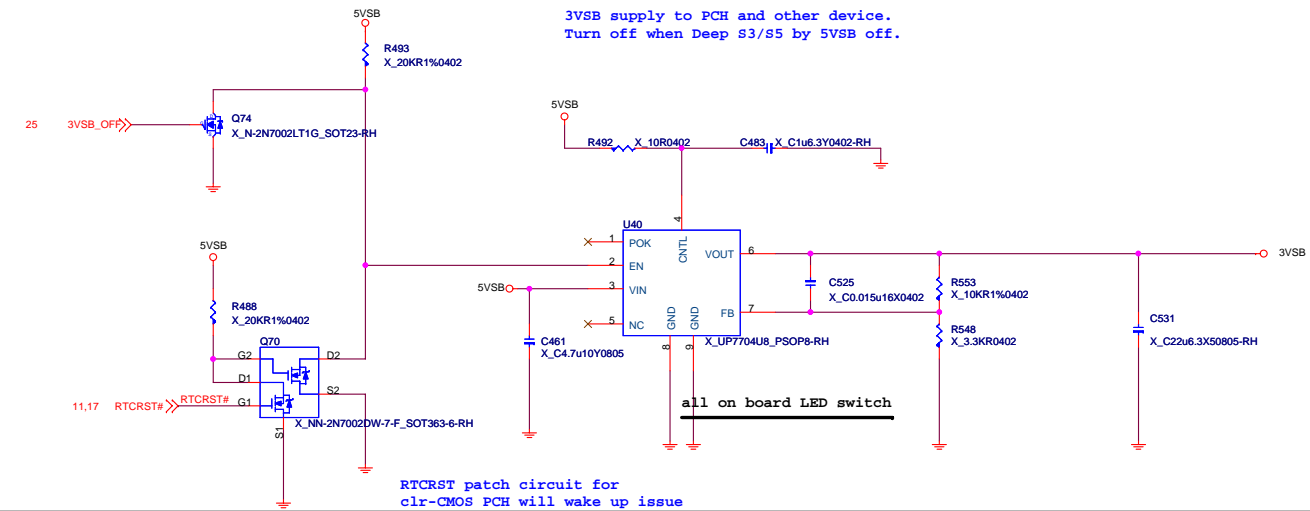
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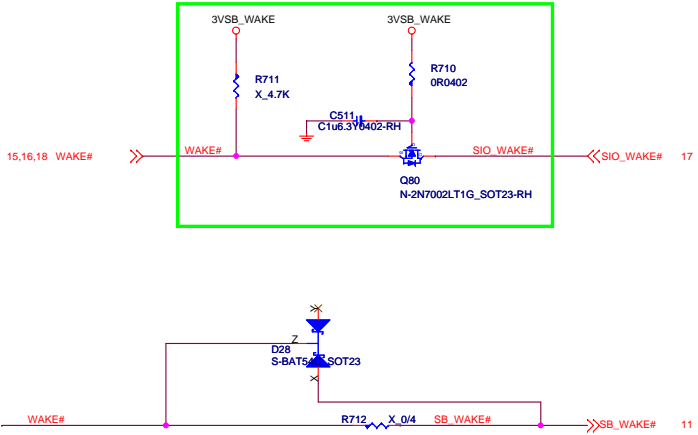
Size	Document Description	Rev
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Deep Mode WOL LAN Power CTRL Circuit

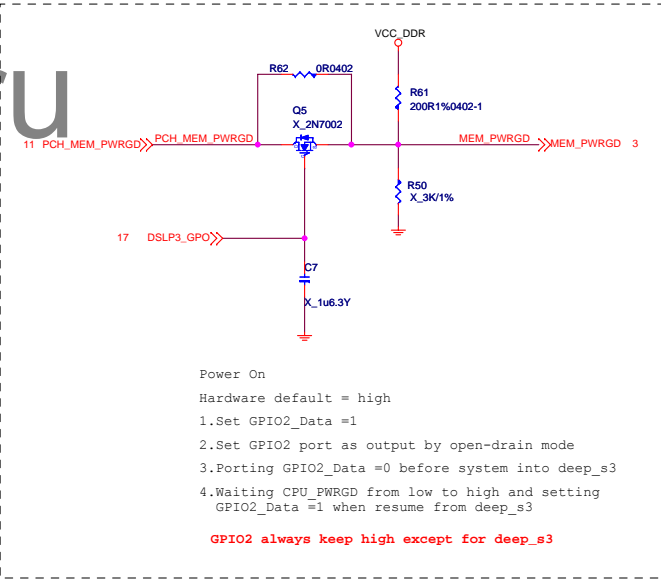


LAN/PCIE/PCI Wake Up CTRL Circuit



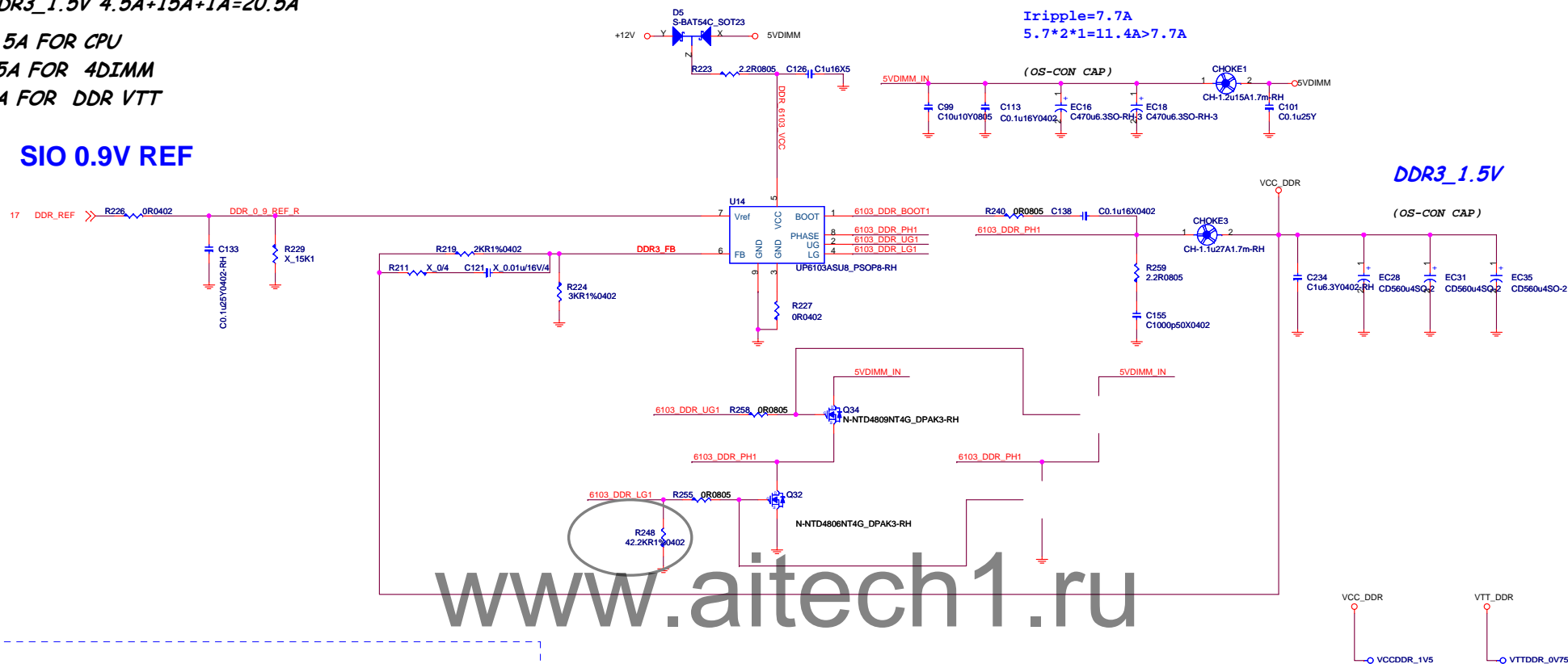
APS & LED

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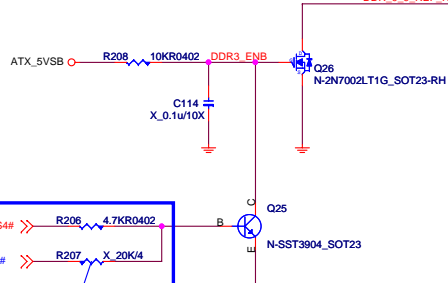


4.5A FOR CPU  
15A FOR 4DIMM  
1A FOR DDR VTT

**SIO 0.9V REF**

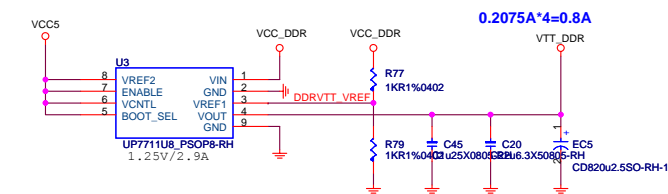


DDR\_0\_9\_REF\_R



### For Deep\_S3 Mode

To CPU Copper trace width > 250mils , Fill island behind DIMM > 400mils .



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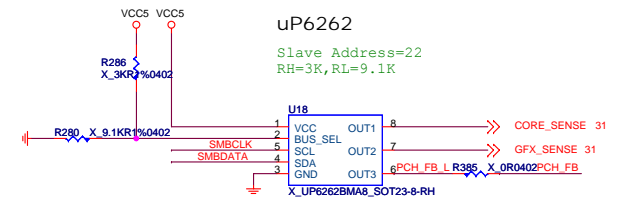
**MS-7680**

Size Custom	Document Description <b>DDR Power - uP6103 1-Phase</b>
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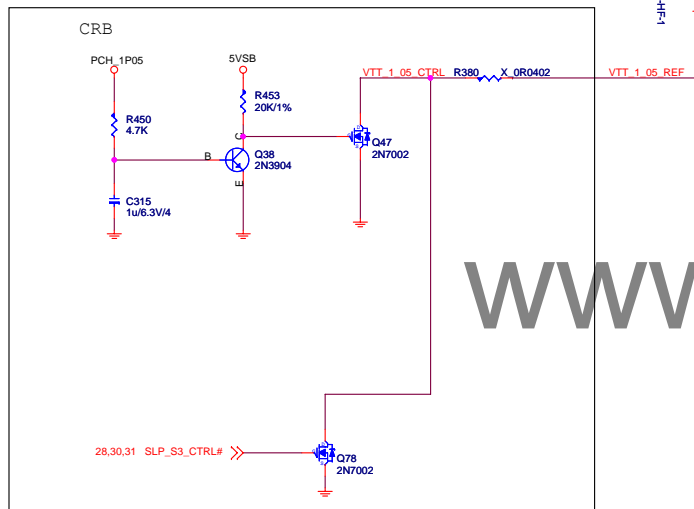
Date: Thursday, October 21, 2010	Sheet 27 of 40
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### 1.8A FOR ME CORE

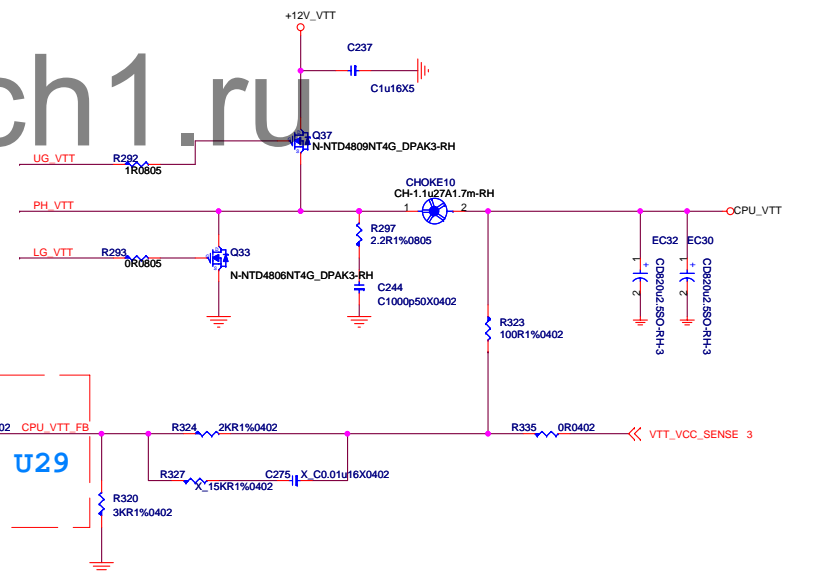
**SIO 0.9V REF**



**CPU VTT 8.5A**  
**8.5A FOR CPU**



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CLose to U29

2 If use SIO ref, R356 should be 20K (R11-0203T12-W08)

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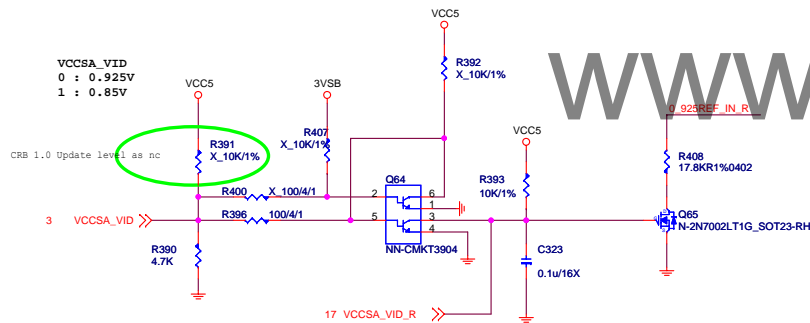
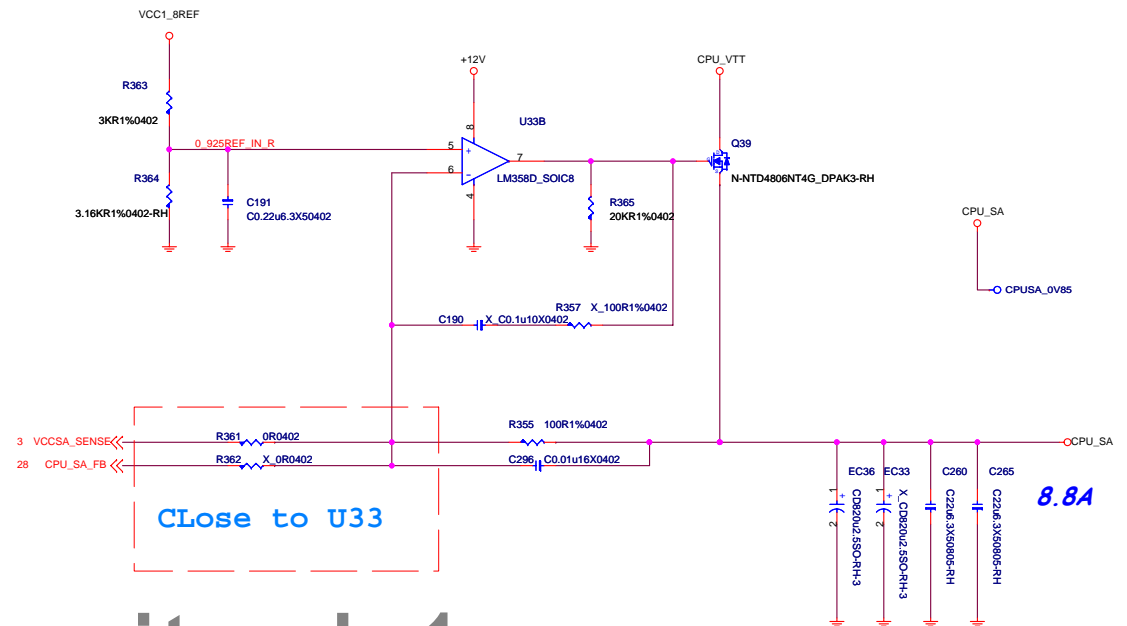
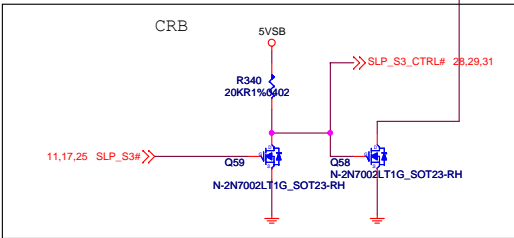
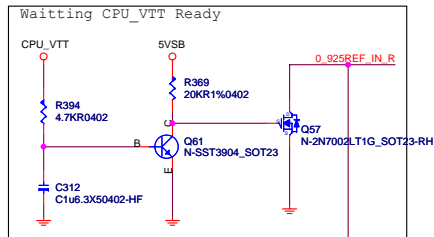
Rev	10
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CPU\_SA:0.925/0.85

SA Core =8.8A



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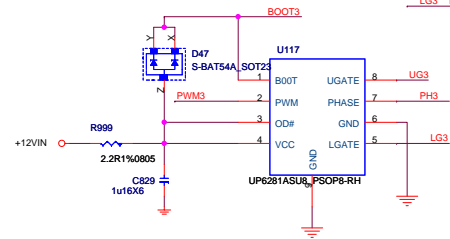


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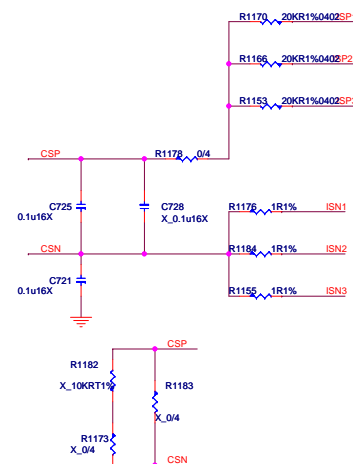
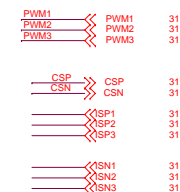
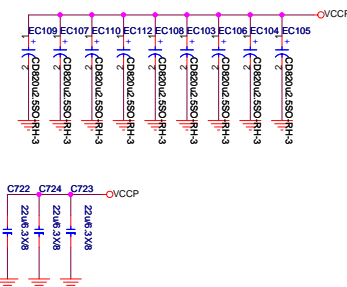
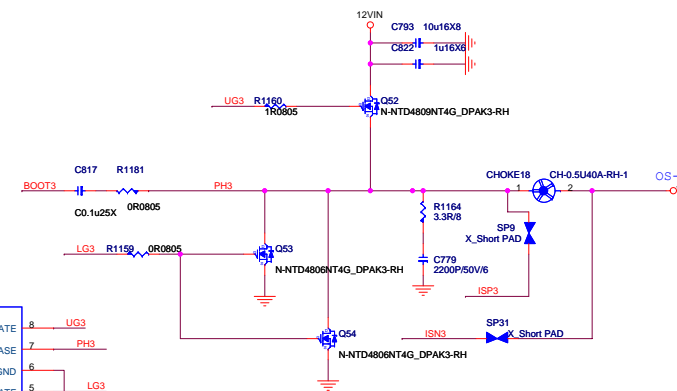
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Custom	CPU_SA - uP6103 1-Phase	10
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VCORE 112A TDC:85A  
LL:1.7m ohm



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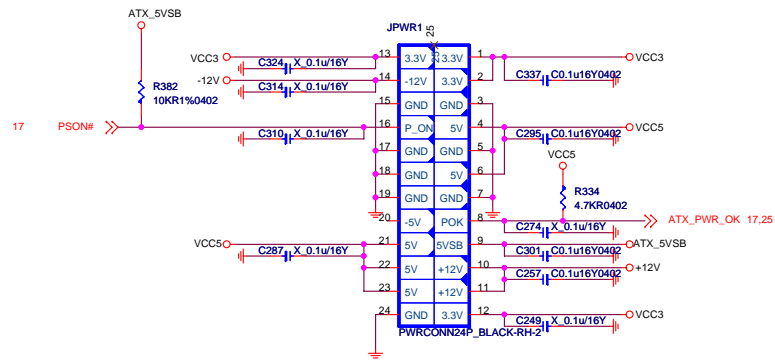
Size Custom	Document Description <b>UP6234 6-Phase CPU</b>
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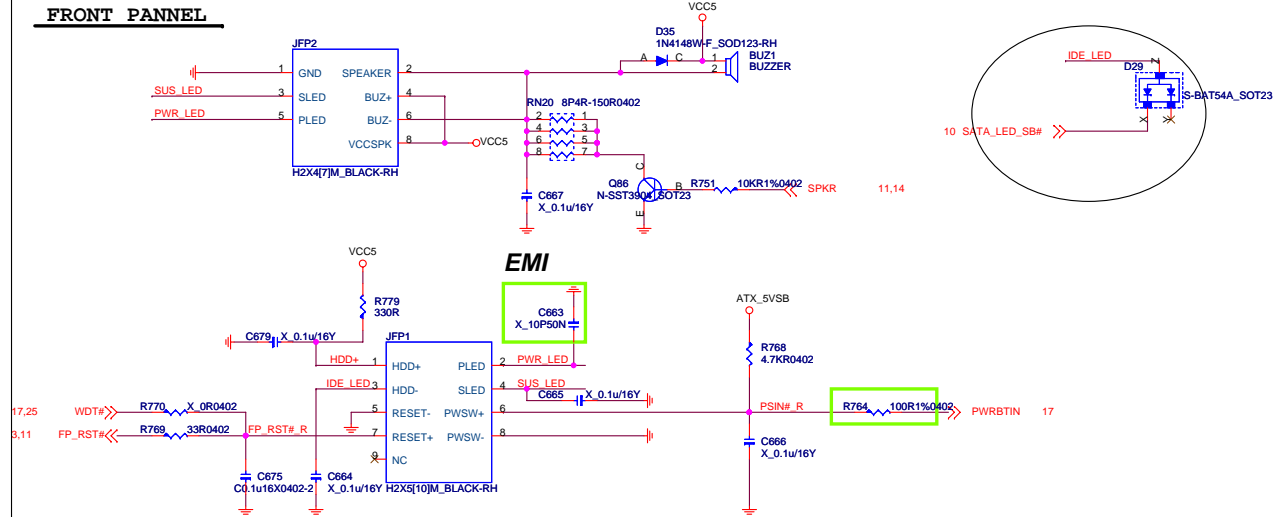
Rev



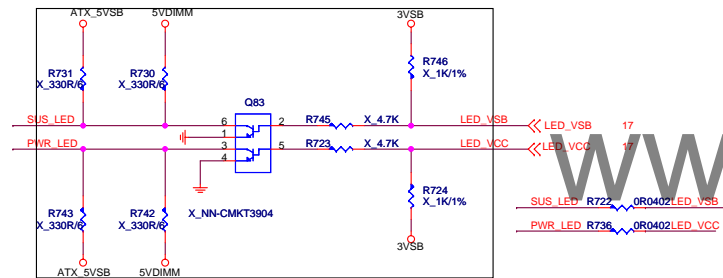
## ATX POWER CONNECTOR



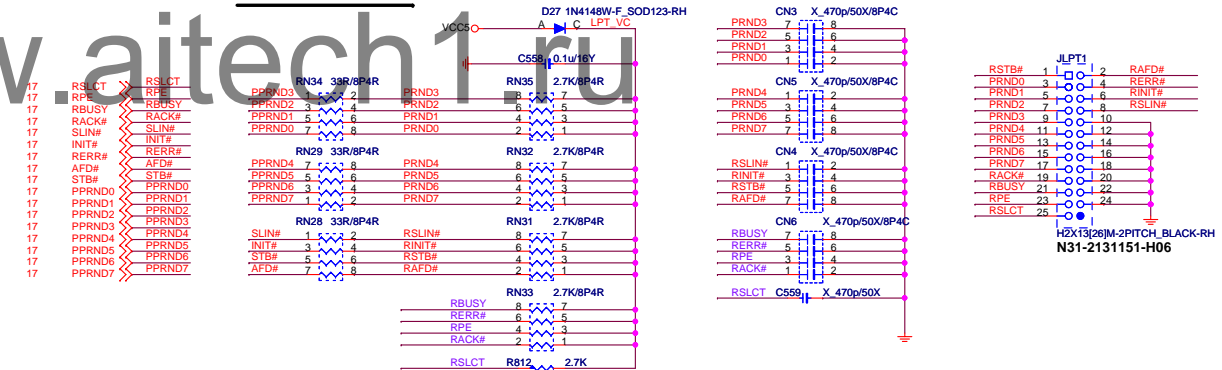
## FRONT PANNEL



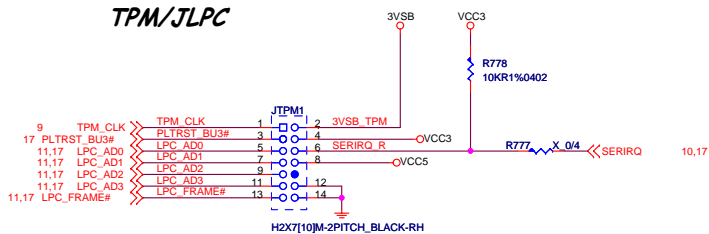
## LED ( for Fintek 71889)



## PARALLAL PORT



## TPM/JLPC

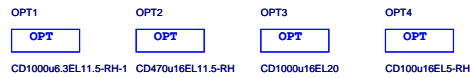
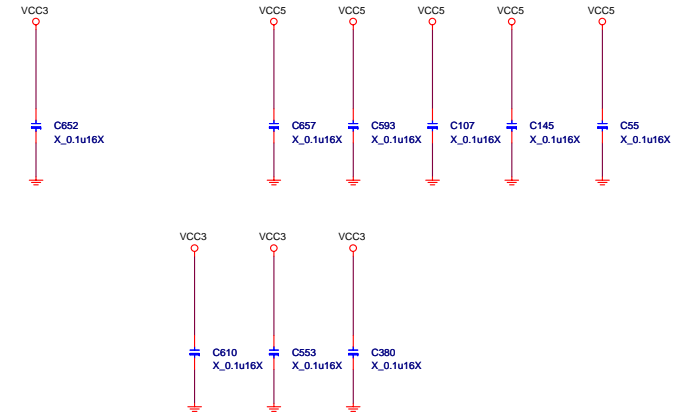


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Custom	ATX PWR-Connector & Front Panel & EMI	10
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# PCH XDP



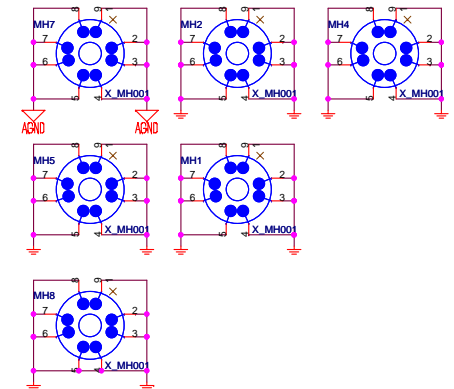
## PCH XDP PWRGD/RESET

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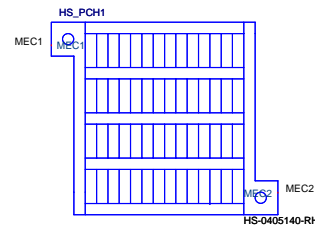
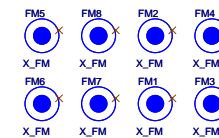
### Simulation



### Mounting Holes



### Optical Fiducial Marks-120



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MS-7680		
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